ACCORING®

38610	YELLOW
38611	BLACK
38612	LIGHT BLUE
38613	DARK BLUE
38614	LIGHT GRAY
38615	LIGHT GREEN
38616	DARK GREEN
38617	TANGERINE
38618	RED
38619	EXECUTIVE RED

WITH WATER RESISTANT
PRESSTEX® COVERS

ACCO INTERNATIONAL INC.
CHICAGO, ILLINOIS 60610

PLANTRONICS
Wilcom

SERVICE MANUAL
MODEL T222C
SIGNALLING TEST SET

wilcom

wilcom products, inc., laconia, n.h.
BOX 508 • D.W. HIGHWAY 03246 U.S.A.
TEL. 603/524-2622 TWX 510-298-1120

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MODEL T222C
SIGNALLING TEST SET

1.0 GENERAL

1.1 Description

1.1.01 The T222C is a portable, general purpose signalling test set, primarily designed to test signaling systems which transmit information in a serial mode. Included in this group are DC systems such as loop, E&M, etc., and one tone system, which is "Single Frequency" or SF system.

1.1.02 Included in the T222C are independently functioning send and receive sections, each with its own circuits which provide the proper line interface according to the type of supervision selected.

1.1.03 The set may be used either as a portable with a carrying case and cover, or as a rack mounted instrument without the portable carrying case.

1.1.04 Either instrument may be operated from 115V or 230V ac 50 to 60 Hz, or optionally operated from 48V central office battery.

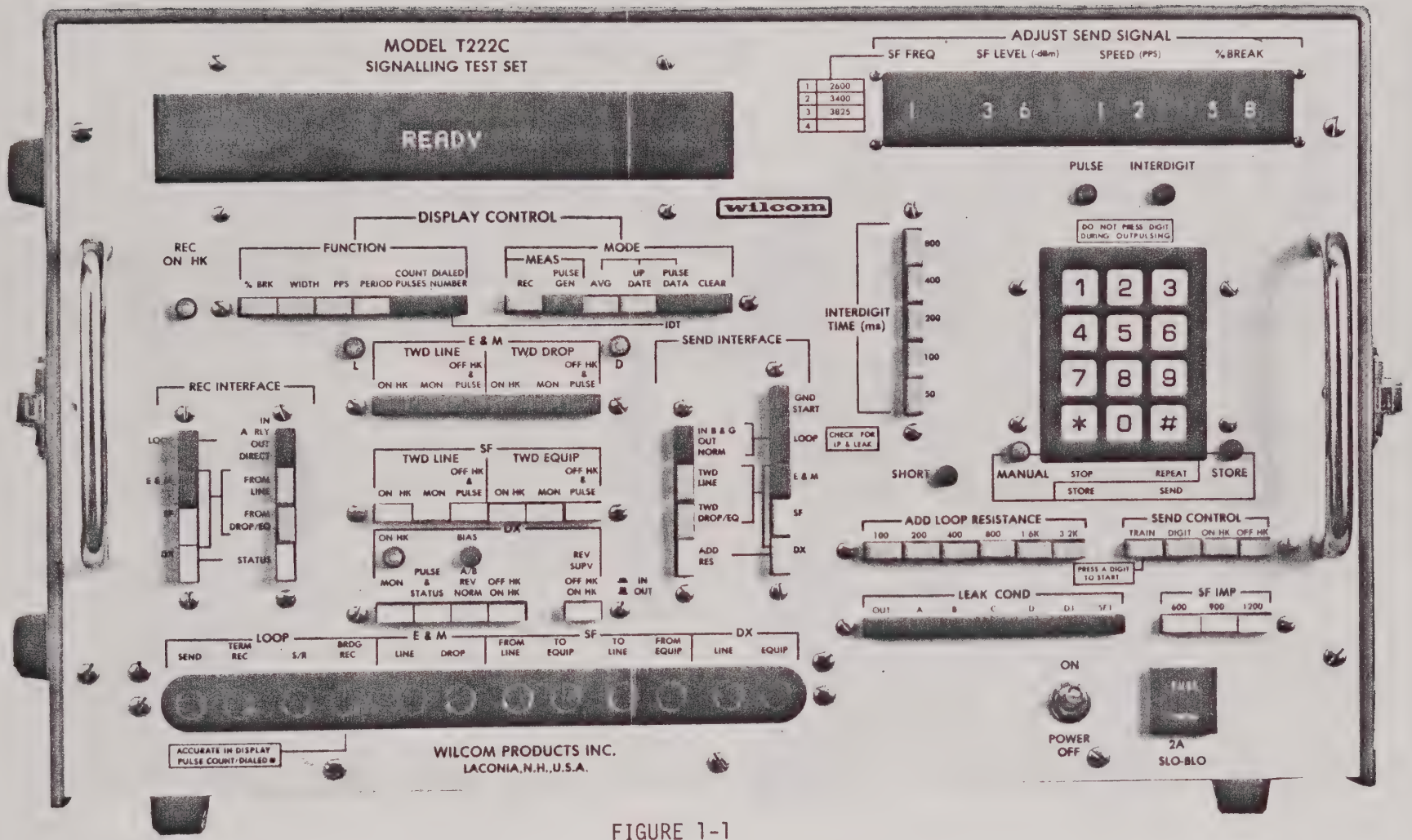


FIGURE 1-1

MODEL T222C
SIGNALLING TEST SET

2.0 SPECIFICATIONS

2.1 Receive Section

2.1.01 Modes of operation: Loop, E&M, DX and SF.

2.1.02 Range of Measurements (IN AVERAGE MODE)

Speed:	2 pps to 50 pps; ±0.2 pps
% Break:	20% to 90% @ 25 pps; ±0.2% (Terminating)
Pulse Width:	3 ms to 599.9 ms; ±0.2ms (Terminating)
Period:	5 ms to 999.9 ms; ±0.2ms (Terminating)
Pulse Count:	up to 9999 pulses at 150 Hz rate

2.1.03 Additional SF Tone Measurements when steady ON HOOK is received.

SF tone level:	0 to -39 dBm (900 ohm) Accuracy ±1 dB
SF tone frequency:	1000 to 3825 Hz

2.1.04 Measuring Circuit Resistance

Loop Signaling 400 ohms;	> 60,000 ohms bridging
E&M Signaling 470 ohms;	> 20,000 ohms bridging
SF Signalling 600 ohms;	> 100,000 ohms bridging
DX Signaling 370 ohms;	> 100,000 ohms bridging

2.1.05 Interdigit Interval

All Modes: must be greater than five times the received pulse width.

2.1.06 "A Relay" Simulation

Resistance:	200 ohms each side
Inductance:	6 H each side; 14 H total @ 60 Hz

Adjusted to 60% at 12 pps; 1200 ohms loop resistance with Leak A.

2.2 Send Section

2.2.01 Range of Pulsing:

Pulse Speed:	0 to 29 pps
% Break:	0 to 99%
Interdigit Interval:	50 to 1550 ms ± 3 ms
SF Level:	0 dBm to -39 dBm @ 600, 900, 1200 ohms; ±.5 dBm (over range & impedance)
SF Frequency:	2600,3400 and 3825 Hz ±2 Hz, <2% THD

2.2.02 Leak Conditions:

A, B, C, D, D1, SF1

2.2.03 Send Circuits:

LOOP (DRY)	25 ohms + ADD LOOP RES switches Current limited to approximately 150 mA
LOOP (B&G)	300 ohms + ADD LOOP RES switches
E&M	Less than 25 ohms Current limited to approximately 150 mA on M lead; E lead current 200 mA maximum
DX	370 ohms + ADD LOOP RES switches
SF	600, 900, 1200 ohms, switch selectable.

2.2.04 Send Functions

Continuous train of pulses
Single digit
Stored Digits (Max. of 16)
Continuous repeating of one digit
Push button dialing of digits
Steady ON HOOK
Steady OFF HOOK

2.3 Environmental

Operating Temperature Range:	0 °C to 50 °C
Humidity:	95% at 35 °C 40% at 50 °C
Storage Temperature:	-40 °C to 75 °C
Altitude (non-operating):	30,000 feet

2.4 Standard Power Input

95 - 135V or 200 - 260V ac 50/60 Hz, switch selectable on rear panel.

50 watts maximum
Fused for 2 amperes

2.5 Optional Power Input

44 - 52.5 dc Central Office Battery

1 1/2 amperes maximum

Not fused

2.6 Mechanical

Portable Unit - 18" W x 10" H x 14" deep, including cover
Weight - 30 lbs. Specify T222C when ordering.

Rack Mounted Unit - 19" W x 10" H x 12" deep
Weight - 25 lbs. Specify T222CR when ordering.

3.1 General

3.1.01 This section describes the functions of each switch, lamp and jack located on the front panel of the Model T222C. This description will be broken down into various sections which relate to power, sending and receiving, and interface selection.

All the push buttons on the front panel are color coded for ease of user operation. The grey buttons are used for all modes of operation. These are used to select such functions as PPS, PERIOD, direction of pulsing or receiving, etc. The green buttons select special functions that will override the functions selected under the grey code. All black buttons apply to functions selected for use in LOOP sending or receiving. The blue buttons are used for selection of E&M functions. The white buttons are used for SF and the cream are used for DX.

3.1.02 Push button action definitions --

(1) Push-push: The switch remains engaged when pressed and must be pressed again to release. The switch function continues as long as the switch remains engaged.

(2) Push-push with lockout: Has the same effects as the push-push action for individual switches except that related switches cannot be engaged simultaneously.

(3) Interlocking: Consists of a group of two or more switches. When any switch in a group is pressed, it automatically releases any other switch that was engaged. The switch function continues until released by pressing another switch in that group.

(4) Interlocking with lockout: Has the same effects as the interlocking action except that no two interlocking buttons may be pressed at one time.

(5) Momentary: The switch remains in only as long as it is pressed. The switch returns to its original position as soon as pressure is removed.

(6) Engaged: The "in" or low profile position.

(7) Released: The "out" or high profile position.

3.2 Input/Output Connections

3.2.01 ac Power Receptacle -- This is a 3-prong male jack recessed in the rear panel of the test set. The line cord supplied with the test set supplies ac power to the test set through this connection. Not part of dc powered T222C.

3.2.02 115/230 Switch -- This switch allows the selection of either 115V primary voltage or 230V primary. The switch is located just under the ac Power receptacle on the rear panel. Not part of dc powered T222C.

3.2.03 Ground Binding Post -- On the rear panel near the center is a 5-way binding post which may be used to supply office ground if required. The set is normally grounded through the ac power cord. If the ground is not supplied through the power cord, the Ground Binding Post must be used to supply signal ground. Not part of dc powered T222C.

3.2.04 Vdc Terminal Strip -- This terminal strip provides connections for power on the 48 Vdc powered T222C. The SIG terminal provides the connection for the -48 Vdc used for line signaling functions while the PWR terminal provides the connection for -48 Vdc test set power.

3.2.05 Fuse -- The snap-action fuse holder is located on the lower right hand corner of the front panel. The 2A slow blow fuse provides the protection for the 115/230 volt ac and the -48 vdc PWR inputs.

3.2.06 Power Switch -- A toggle type power switch is used as the on-off switch for powering the set. The switch is located just to the left of the fuse holder.

3.2.07 Jack Field -- The lower left corner of the front panel has a field of 12 jacks. The jacks are used to make connections to the circuit to be tested. The jacks are all W.E. Type 310. The field is further broken down into 4 sections, LOOP, E&M, SF, and DX. The jacks under each section are used to make connections to circuits under test for related types of pulsing only; for example, the TERM REC Jack under the LOOP section is used only for Loop type signaling.

3.2.08 Loop Jacks -- On the most left hand side of the jack field are 4 jacks under the bracket designated LOOP. These jacks are used for making connections to the Loop pulsing circuits.

1. SEND — This jack is used for connecting a circuit where Loop pulsing is required. The tip and ring supply either Loop closures, Battery and Ground pulsing or Loop Closures with Ground Start depending on selection of Send Interface Controls.

2. TERM REC — This jack is used for all terminated Loop receiving. The tip and ring are connected to either the simulated A relay or through a resistive battery feed for direct measurements. The selection of different receive modes is in response to the Receive Interface Controls.

3. S/R — This jack has the tip and ring connected in parallel with the Send jack, the sleeve is connected to the battery referenced side of the loop receiver so ground and open pulsing may be detected. The jack has uses in the testing of some pulse repeating relays and toll test pulsing requirements.

4. BRDG REC — This jack is used to make measurements on a working loop on a bridging basis. When a plug is connected into this jack the other loop receivers are overridden so this jack must be vacant if the TERM REC jack is to be used. Any circuit that is connected to this jack must have dc supervision (wet loop) in order for the Bridging Receiver to work. The BRDG REC jack is intended to be used for dialed number or pulse count display.

3.2.09 E&M Jacks -- Just to the right of the Loop jacks are two jacks designated LINE & DROP.

1. LINE Jack — This jack is to connect to the line side of the E&M circuit. The M lead pulser is on the ring of this jack and the E lead detectors are on the tip of this jack.

2. DROP Jack — This jack is used to connect to the Drop side of an E&M circuit. The E lead pulser is on the tip of this jack and the M lead detectors are on the ring of this jack.

3.2.10 SF Jacks -- These four jacks are located under the bracket designated SF. These are used - in pairs - to make connections to the SF circuit. The FROM LINE and TO EQUIP jacks are the receive side jacks or the +7 TLP jacks. The other pair, TO LINE and FROM EQUIP are transmit side or the -16 TLP.

3.2.11 DX Jacks -- The last two jacks are used to connect to the DX (Duplex Signaling) system. In a dc signaling circuit the closest DX set is designated the EQUIP side and the more distant DX set is the LINE side.

1. LINE — This jack is used to connect into the circuit toward the more distant DX set. The tip is the A lead and the ring is the B lead.

2. EQUIP — This jack is used to connect into the circuit toward the closer of the two DX sets.

3.3 Pulse Generator Controls

3.3.01 The controls which are used to initiate the outpulsing are located on the right hand side of the Test Set. These controls are used to set the characteristics of the outgoing pulsing.

3.3.02 ADJUST SEND SIGNAL -- On the upper right corner of the set are three sets of thumbwheel switches, two of which are labeled SPEED (PPS) and % BREAK. These two sets of thumbwheel switches are used to select the characteristic of the sending signal. The SPEED thumbwheels select pulses per second from 1 to 29 in one pps increments. The % BREAK thumbwheels adjust from 1 - 99% BREAK. If 0 pps or 0% BREAK is selected the pulse generator does not function since this condition is equivalent to a steady off hook.

3.3.03 Keyboard -- The keyboard is a 3 by 4 matrix with digits 0 - 9 and two special function keys; the "*" and the "#". Two modes of operation for sending digits are available; a MANUAL mode and a STORE mode. The mode is changed by pressing "*" for 2 seconds and is indicated by one of two LEDs.

a. In the MANUAL mode, digits are immediately outpulsed as they are entered. Pressing "#" will result in the previous entry being repeated continuously with a delay between digits equal to the setting on the INTERDIGIT time switch. A new digit may be entered during outpulsing while the interdigit light is on.

b. In the STORE mode, any number of up to 16 digits may be entered on the keyboard. The entire stored number is outpulsed when "#" is pressed and may be repeated as many times as desired. Before storing a new number, the "*" key should be pressed once to clear internal counters.

3.3.04 INTERDIGIT TIME (ms) -- the send interdigit time is set on the INTERDIGIT TIME (ms) push buttons; the settings are additive. The send interdigit interval is programmable from 50 ms to 1550 ms in 50ms increments.

3.3.05 SEND CONTROL:TRAIN,DIGIT,ON HK,OFF HK -- Four push buttons having interlocking withlockout action are used to select the output mode of the Pulse Generator. With the SEND CONTROL:TRAIN button engaged, gaged the Pulse Generator continuously generates pulses characteristic of the SPEED and % BREAK thumbwheel settings. The train of pulses is initiated by pressing any digit (0-9) while in the MANUAL mode. With the SEND CONTROL:DIGIT button engaged, the Pulse Generator pulses are determined by the SPEED and %BREAK thumbwheel settings and the keyboard inputs. With the ON HK button engaged the Pulse Generator output is steady On Hook; with the OFF HK button engaged, the Pulse Generator output is a steady Off Hook (idle).

3.3.06 PULSE & INTERDIGIT Lamps -- The Pulse Generator section has two indicator Lamps. These lamps, when lighted, indicate the operational status of the Pulse Generator. The PULSE Lamp, which is a green LED, indicates when the Pulse Generator output is in the on hook condition. The INTERDIGIT Lamp, which is a red LED, indicates the interdigit interval.

3.4 Display & Display Controls

3.4.01 The Display and Display Controls are located in the upper left hand corner of the Test Set.

3.4.02 The display is a 32 character alphanumeric device, capable of displaying a full 64 character ASCII subset. It is used to display all of the measured parameters as selected by the FUNCTION and MODE controls. Appropriate labels -- such as; 60% BRK, 8 PULSE, 100.1 PER — are added to the measured values to help identify what is actually being measured.

3.4.03 DISPLAY Controls -- The Display Controls are located directly underneath the Display and are broken down into two groups, FUNCTION and MODE.

3.4.04 FUNCTION:DIALED NUMBER,COUNT PULSES — Under the FUNCTION grouping, the priority button is the DIALED NUMBER; selection of this button supersedes any other selection in this group. In this mode the display presents the digits as dialed. Up to 26 digits can be entered and displayed. After receipt of an entire dialed number, the interdigit intervals for the first sixteen received digits can be displayed by repetitive presses of the MODE PULSE DATA button. Interdigit Times of greater than 3999 msec. will be displayed with an over-range indicator (>3999). The next button, labeled COUNT PULSES, has the next level of priority. This button which has lockout with the DIALED NUMBER button, causes the test set to display the updated pulse count continuously as received through the receive interface. When COUNT PULSES is selected, the count accumulates from the time the CLEAR button is pressed, or from the time the word READY appears on the screen, until the CLEAR button is engaged again.

3.4.05 FUNCTION:% BRK, WIDTH, PPS, PERIOD — With the COUNT PULSES and DIALED NUMBER buttons both released, then the control of the display function reverts to selection of % BREAK or WIDTH, which are interlocked with each other, and the PPS or PERIOD buttons, which are also interlocked with each other. If no buttons are engaged (of these four), then % BREAK and PPS are displayed. To avoid confusion, each entry into the display is labeled with its appropriate function.

3.4.06 MODE — Under the DISPLAY CONTROL to the right are a group of buttons caled MODE. These buttons select the mode in which the previously selected functions will be displayed.

3.4.07 MODE:MEAS:REC, PULSE GEN — These two interlocked buttons select the source of the pulsing input to the measuring circuits. When the REC button is engaged, the pulsing from the receive interface is selected. When the PULSE GEN button is engaged, the measuring circuit input is connected to the output of the pulse generator without interrupting the pulsing to the Send Interface. The PULSE GEN button may therefore be used to verify the pulse generator operation during actual pulsing of a circuit.

3.4.08 MODE:AVG, UPDATE — These two buttons are interlocked. The AVG button causes the Test Set to display a reading averaged over a number of incoming pulses. Normally this number is 9 and is obtained by having the far end pulse ten pulses or a continuous pulse train in which case the Test Set averages every 10 pulses, continually updating every tenth. The UPDATE mode causes the set to display the measured parameters of each pulse as it comes in.

NOTE: In the AVG or UPDATE mode, a minimum of two pulses must be received to display any parameters. In the AVG mode, if fewer than ten pulses are received, the Test Set averages the number of pulses received minus one. If 8 pulses are received, the first seven pulses are averaged.

3.4.09 MODE:PULSE DATA — This momentary action button performs two functions. In the DIALED NUMBER DISPLAY mode, pressing PULSE DATA will result in a display of the interdigit time between the received digits (up to 16). In % BRK, PPS, WIDTH and PERIOD display modes, pressing PULSE DATA will result in a display of the selected parameters (i.e., % BRK and PPS) for each pulse in a received digit. In addition, the data may be re-displayed in terms of any of the four pulse parameters by selecting the desired parameters and repetitively pressing PULSE DATA.

3.4.10 MODE:CLEAR — This button is a momentary type action. The CLEAR button may be pressed at any time, and results in a return of the Test Set to intial conditions with all registers clear and the word READY on the display. Operation of the CLEAR button has no affect on the sending of pulses; it affects only receive data.

3.4.11 REC ON HK Lamp -- This lamp, a red LED, is located to the left of the DISPLAY CONTROL buttons. This lamp when lighted indicates an On Hook is being received from the selected interface. The lamp is also a visual indication of pulsing that is being sent to the Measuring Circuits for display. If the REC ON HK lamp is not pulsing, then the Measuring Circuits are not receiving any pulses for display.

3.5 SEND INTERFACE Controls

3.5.01 General -- The Send Interface buttons are two vertical columns of four and five buttons each near the center of the front panel. These buttons select the type and direction of outpulsing.

3.5.02 SEND INTERFACE CONTROLS:GROUND START,LOOP,E&M,SF,DX — These five buttons are interlocked with lockout and are used to select the type of outpulsing. Further description of these controls is given in each operational section.

3.5.03 SEND INTERFACE CONTROLS:B&G/NORM,TWD LINE,TWD DROP/EQ,ADD RES - The B&G/NORM button is a push-push type and selects either Battery and Ground or normal loop closures for loop pulsing. The TWD LINE and TWD DROP/EQ buttons are interlocked and select the sending direction for the pulsing. The ADD RES is a push-push type used in DX to add loop resistance in the pulsing output.

3.6 REC INTERFACE Controls

3.6.01 The Receive Interface Controls are on the left hand side of the panel and are made up of two vertical columns of four buttons each. These are used to select the type of interface to receive the pulsing.

3.6.02 REC INTERFACE:LOOP,E&M,SF,DX -- These four buttons are interlocked with lockout and are used to select the type of interface for receiving. More specific information will be covered in each operational section.

3.6.03 REC INTERFACE:"A" RLY/DIRECT,FROM LINE,FROM DROP/EQ,STATUS - The "A" RLY/DIRECT button is a push-push type and is used to select either the simulatd "A" type relay mode or the direct mode of loop measurement. The FROM LINE and FROM DROP/EQ buttons are interlocked and are used to select the direction from which the pulses are received. These last two buttons also control the receive thresho 0lt of the SF receive interface.

STATUS is a momentary type button and is used in the DX mode to determine the correct orientation of the A & B Leads.

3.7 Supervision Controls

3.7.01 Between the Send Interface and Receive Interface buttons are three groups of horizontal buttons. These buttons are the supervision controls and are used to establish the supervision each interface provides its associated jacks. The top group of six buttons are used for E&M supervision; the middle six buttons are used for SF supervision; and the bottom five buttons are used for DX supervision. The buttons will be further explained in each operational section.

3.8 Misc Send Controls

3.8.01 ADD LOOP RESISTANCE — Six push-push type buttons are used to select the amount of loop resistance to be added to the output of either the loop pulser or the DX pulser. Engaging the buttons adds the amount marked above the button to the output with one half in the ring and the other half in the tip. For example, if the 800 button is engaged the tip has 400 ohms and the ring has 400 ohms.

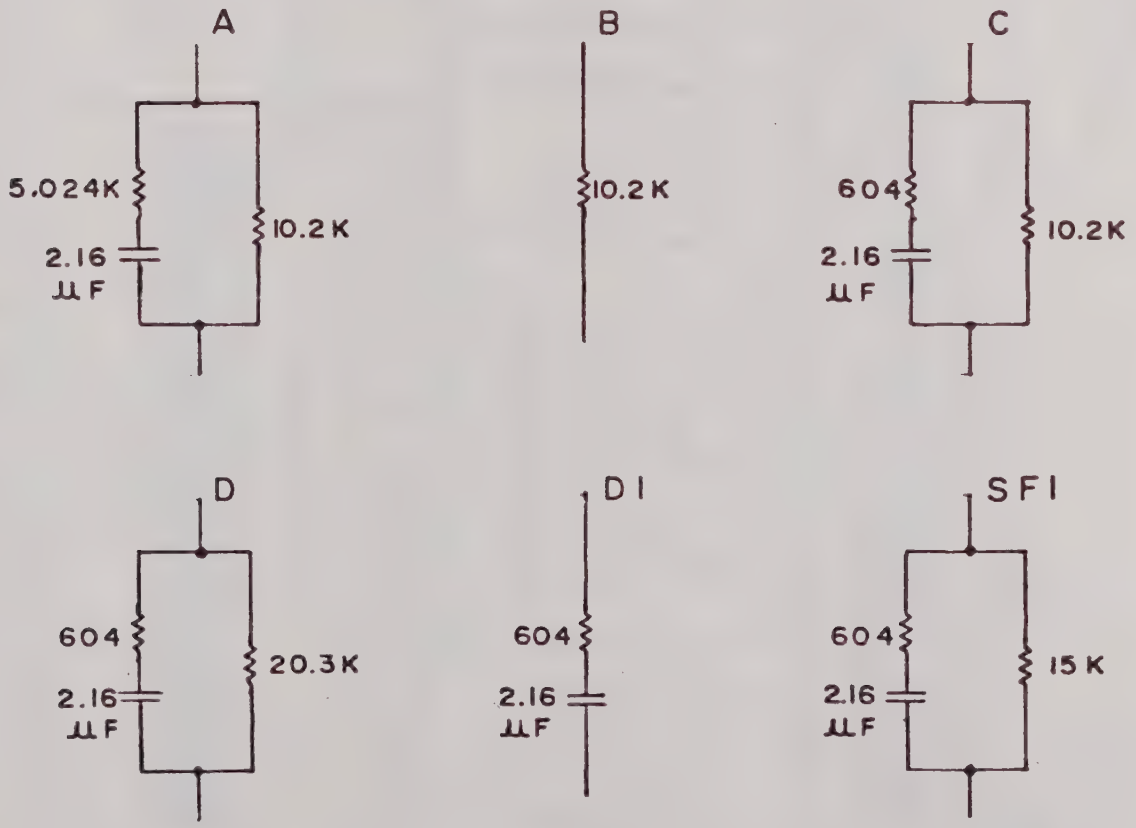
3.8.02 SF IMP — These three buttons are interlocked and are used to select the output impedance of the SF interface.

3.8.03 ADJUST SEND SIGNAL:SF LEVEL — The SF level thumbwheel switches set the output level of the SF to be sent. The switches are located in the upper right hand corner of the front panel.

3.8.04 ADJUST SEND SIGNAL:SF FREQ — The SF FREQ thumbwheel selects one of three or an optional 4th frequency for SF send functions.

3.8.05 SHORT Lamp -- The SHORT lamp which is located just above the ADD LOOP RESISTANCE buttons is used to indicate when excessive current is being drawn by a sending circuit, for example, a ground on the M lead.

3.8.06 LEAK COND — The six buttons marked A thru SF1 are interlocked and the OUT is a push-push type action. The leak conditions are used in the loop pulser only. Send leak conditions are shown below. More information is in the Loop Section.



T222C LEAK CONDITIONS

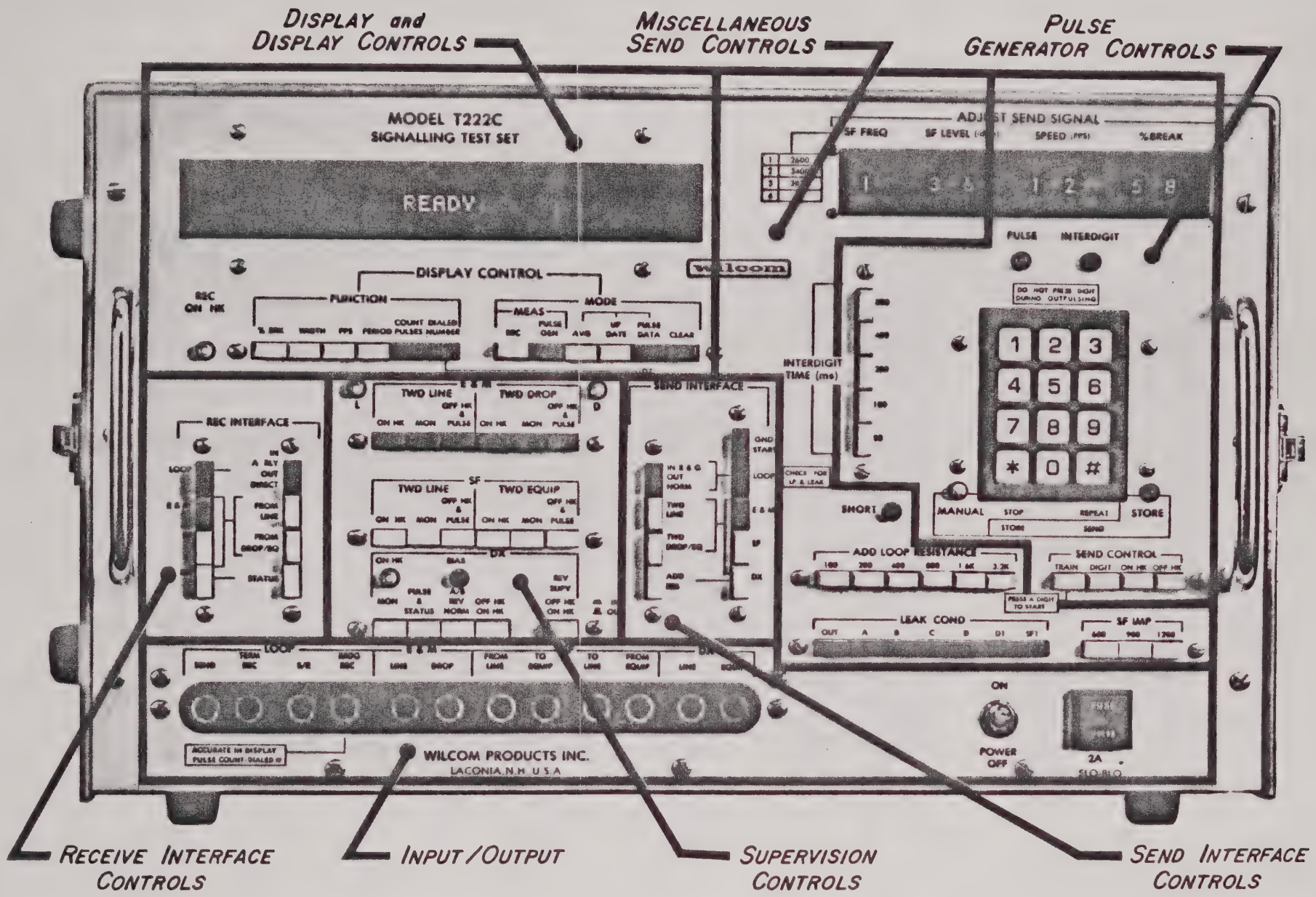


FIGURE 3-1
PANEL CONTROLS AND CONNECTIONS

4.1 ac POWER

4.1.01 The T222C is powered by either 115 or 230 volts ac. For operation, connect the line cord to the recessed male connector on the rear panel and set the voltage slide switch for the line voltage which is being used. Power is supplied to the Test Set by placing the POWER toggle switch in the ON position.

4.1.02 The Test Set is ready for operation as soon as power is applied. Detailed operation information is obtained by refering to the appropriate portions of Section 3 and Section 4.

4.2 dc POWER

4.2.01 When the T222C is equipped with the dc power option, -48 Vdc is connected to the SIG and PWR terminals on the rear panel. The GND terminal is connected to office ground. Power is supplied to the Test Set by placing the POWER toggle switch in the ON position.

4.2.02 The front panel fuse provides protection for the -48 Vdc PWR input terminal. The -48 Vdc SIG input terminal is not fused.

4.3 DISPLAY CONTROLS

4.3.01 The two buttons MEAS:REC/PULSE GEN, select the source of the pulsing to be measured. When the REC button is engaged, the pulsing from the REC INTERFACE is measured. When the PULSE GEN button is engaged, the output of the pulse generator is measured without interrupting the pulsing to the SEND INTERFACE.

4.3.02 The remaining ten DISPLAY CONTROLS provide six of the seven status inputs to the Central Processing Unit (CPU) to control the computation and display functions (the seventh is provided by the REC INTERFACE:SF button). Detailed functional descriptions are provided in Section 3.4 for each push button.

4.3.03 The CLEAR button, when pressed, initializes the status of the CPU. If CLEAR is pressed during a pulse train while the set is actively engaged in measuring, the set immediately returns to the measurement mode that it left when the CLEAR button was pressed. However, all previously stored data such as PULSE DATA, COUNTPULSES, etc., are erased and begin accumulating anew from that point.

4.3.04 When the Test Set is operating in the AVG or UPDATE mode, a minimum of two pulses must be received to display any parameters. In the AVG mode, if fewer than ten pulses are received the Test Set averages the number of pulses received minus one, i.e., if eight pulses are received, the first seven pulses are averaged.

4.3.05 If fewer than two pulses in UPDATE or fewer than three pulses in AVG mode are received the set returns to ready.

4.4 PULSE GENERATOR

4.4.01 The Pulse Generator controls determine the characteristics of the pulsing provided to the SEND INTERFACE controls for outpulsing. A crystal controlled time base is used in the pulsing circuits for high accuracy.

4.4.02 When either the E&M or the SF Supervision Control push button labeled OFF HK & PULSE is engaged, outpulsing is controlled by the Pulse Generator controls. These include:

1. SEND CONTROL
2. Keyboard (Manual - Store)
3. INTERDIGIT TIME (ms)
4. ADJUST SEND SIGNAL
   (a) SPEED (PPS)
   (b) % BREAK

4.4.03 The four SEND CONTROL push buttons (TRAIN, DIGIT, ON HK and OFF HK) each send a series of pulses of the required characteristics to the circuit being tested. The keyboard is used for dialed number entry as well as pulsing control. Two modes of operation are available for sending digits - a MANUAL mode and a STORE mode. In the STORE mode up to 16 digits may be stored and dialed repeatedly. The send interdigit interval (INTERDIGIT TIME) is programmable from 50 ms to 1550 ms in 50 ms increments. Thumbwheel switches are used to control the pulse SPEED from 0 to 29 pps in one pps increments, and the % BREAK from zero to 99% in 1.0% increments.

4.4.04 The various systems for sending a pulsing signal are selected by the SEND INTERFACE which provides Loop, Loop/Ground Start, E&M, SF or DX modes.

4.5 LOOP OPERATION

4.5.01 General -- The Test Set has the provisions for general loop outpulsing and detection. The send section can outpulse on a loop closure or Battery and Ground basis. A momentary action push button applies a ring ground when pressed for ground start operation. The loop detector receives on a terminated or bridging basis. The outpulsing is performed by solid state pulsers which reproduce the operation of relays without the inherent variation in operation. The solid state loop detectors have two types of terminated receivers; the inductor feed simulated "A" relay and the resistive feed direct measurements.

4.5.02 Description of Controls -- This section cover the controls that are used for general loop pulsing and receiving. The controls that are unique to loop are color coded black.

a. REC INTERFACE -- The following two buttons are used for Loop Receiving:

   1. LOOP -- This button connects the output of the selected loop detector to the measuring circuits for display.

2. "A" RLY/DIRECT — This button selects the type of terminated receiver connected to the TERM REC Jack. When engaged, a receiver that simulates the operation of an "A" relay is connected to provide displayed readings based on the performance of a typical "A" relay. When released, a direct measuring receiver is connected to provide displayed readings of the actual signaling (open and closed) durations.

b. SEND INTERFACE — The following two buttons are used for Loop Pulsing:

1. GROUND START — This button applies a ground to the ring of the send loop jacks when pressed.

2. LOOP — This button connects the output of the Pulse Generator to the selected loop pulser.

3. B&G/NORM — This button selects the type of pulser connected to the LOOP SEND jack. When engaged, the Battery and Ground Pulser provides battery/open pulsing on the tip and ground/open pulsing on the ring. When released, a solid state device provides loop closures between the tip and ring.

c. ADD LOOP RESISTANCE — The Loop Resistance buttons are located in the lower right hand side of the set. When a button is engaged, the value of the button is added to the loop pulsing circuit. For example, if 1200 ohms is to be added to the loop then the 400 and 800 ohm buttons should be engaged and all the others should be released.

d. LEAK COND — The Leak Condition buttons are located under the Loop Resistace buttons. The Leak Condition buttons are interlocked so only one condition can be selected at a time. To put the condition in the loop pulsing circuit, the OUT button has to be released and the desired LEAK COND has to be engaged. By engaging the OUT button, the leak condition is removed from the circuit.

4.5.03 Bridging Loop Measurements

a. Bridging loop measurements are intended to be used on a circuit only to receive a dialed number or to check the supervision on a circuit without breaking the loop. To make the bridging loop measurements the following button is operated:

ENGAGE

REC INTERFACE:LOOP

b. The bridged circuit is plugged into the BRDG REC Jack. The REC ON HK Lamp shows the supervision or pulsing that is occuring on the circuit. By engaging the DIALED

NUMBER button under the DISPLAY CONTROL the number that is being dialed is displayed. The % BREAK may be displayed but the accuracy is degraded because of various loop conditions. The speed will be displayed with the measuring accuracy of the Loop Detector. The BRDG REC Jack must be vacant for terminated Loop measurements.

4.5.04 Terminated Loop Measurements

a. The T222C makes terminated loop measurements either in a direct reading mode or in a simulated "A relay" mode. To make the terminated loop measurements the following buttons are operated:

ENGAGED
REC INTERFACE:LOOP
REC INTERFACE:"A" RELAY/DIRECT (See Note)

NOTE: The "A" RLY/DIRECT button should be set to the position of the desired type of measurements.

b. The circuit to be tested is connected to the TERM REC Jack. The REC ON HK Lamp indicates the supervision or pulsing of the circuit. The Display Controls should be set for the presentation desired.

4.5.05 Loop Pulsing Measurements

a. Two types of loop pulsing are provided by the test set; normal loop closures, and battery and ground pulsing.

b. Normal Loop (Dry) — To outpulse with loop closures the following buttons are operated:

ENGAGE	RELEASED
SEND INTERFACE:LOOP	SEND INTERFACE:NORM/B&G

1. The circuit to be pulsed is connected to the LOOP:SEND Jack. The LOOP S/R Jack has the same pulsing across its tip and ring. The two jacks are connected in parallel. The outgoing pulses are controlled by the Pulse Generator.

2. Ground Start circuits may be seized by pressing the GND START push button.

c. Battery & Ground -- In order to provide battery and ground outpulsing the following buttons are operated:

ENGAGED
SEND INTERFACE:LOOP
SEND INTERFACE:B&G/NORM

1. The circuit to be pulsed is connected to the LOOP:SEND Jack. The outgoing pulses are controlled by the Pulse Generator.

4.6 SF OPERATION

4.6.01 General -- The SF section of the Test Set interfaces an SF circuit at a 4-wire point in the office. The section has its own synthesizer with outputs of 2600, 3400 and 3825 Hz and is capable of sending SF tone at any of three impedances: 600, 900, or 1200 ohms. The sending level can be varied over the range from 0 to -39 dBm in 1 dB steps. The SF tone can be received in either a high impedance monitoring mode or a terminated 900 ohms mode.

a. When receiving SF pulsing, the Display Controls determine the information displayed on the alphanumeric readout.

b. When tone (ON HOOK) is received for longer than one second without interruption, the Test Set automatically measures and displays the LEVEL and FREQUENCY of the tone. The display measurement is updated every second until the tone disappears (OFF HOOK); at which time the last measurement is held and displayed. Control of the measurement and display automatically reverts to the Display Controls when SF pulsing is received.

4.6.02 Description of Controls -- This section covers controls that are used during SF pulsing or receiving and determine the direction for both operations. Controls which are unique to SF operation are color coded white.

a. REC INTERFACE — The following three buttons are used for SF receiving.

1. SF — This button, when engaged, connects the SF detector output to the measuring circuits for presentation on the display.

2. FROM LINE — This button, when engaged, connects the SF detector to the SF:FROM LINE Jack and switches the SF receive threshold for rejection of tone less than -26 dBm (2600 Hz only).

3. FROM DROP/EQ — This button, when engaged, connects the SF detector to the SF:FROM EQUIP Jack. Also, the receive sensitivity is increased to -40 dBm.

b. SEND INTERFACE — The following three buttons are used for SF pulsing:

1. SF — This button, when engaged, connects the output of the Pulse Generator to the SF Send Interface and Supervision controls.

2. TWD LINE — This button, when engaged, connects the output of the SF Level control circuit to the SF Supervision Controls for gating by the Pulse Generator and connection to the SF:TO LINE Jack. An SF tone at -24 dBm is also connected to the SF Supervision controls to provide reverse supervision to the SF:TO EQUIP Jack.

3. TWD DROP/EQ — This button, when engaged, connects the output of the SF Level control circuit to the SF Supervision Conrols for gating by the Pulse Generator and connection to the SF:TO EQUIP Jack. An SF tone at -20 dBm is also connected to the SF Supervision Controls to provide reverse supervision to the SF:TO LINE Jack.

c. SF Supervision Controls -- The following six buttons, in conjunction with the SEND INTERFACE Controls, determine the type and direction of SF signaling. Two sets of identical buttons control the functions for TWD EQUIP or TWD LINE.

1. The three TWD EQUIP buttons determine the supervision for the SF:TO EQUIP Jack as follows:

ON HK — When this button and the SEND INTERFACE:TWD DROP/EQ button are engaged, and SF tone of the level set on the SF LEVEL thumbwheels is sent on the TO EQUIP Jack. If this button and the SEND INTERFACE:TWD LINE button are engaged, a fixed level of -20 dBm is sent on the TO EQUIP Jack. When the ON HK button is engaged, the SF:FROM LINE Jack is terminated in 600 ohms.

MON — When this button is engaged, the SF:FROM LINE Jack is connected to the SF:TO EQUIP Jack. This allows monitor measurements to be made on the receive path of the SF circuit when the REC INTERFACE:FROM LINE button is engaged.

OFF HK & PULSE — When this button and the SEND INTERFACE: TWD DROP/EQ button are engaged, the tone output of the SF Level control circuit is gated by the Pulse Generator output signal and sent on the SF:TO EQUIP Jack. If this button and the SEND INTERFACE:TWD LINE button are engaged, no tone (OFF HOOK) appears at the SF: TO EQUIP Jack. When this button is engaged, the SF:FROM LINE Jack is terminated in 600 ohms.

2. The three TWD LINE buttons determine the supervision for the SF:TO LINE Jack as follows:

ON HK — When this button and the SEND INTERFACE:TWD LINE button are engaged, an SF tone of the level set on the SF LEVEL thumbwheels is sent on the TO LINE Jack. If this button and the SEND INTERFACE:TWD DROP/EQ button are engaged, a fixed level of -20 dBm is sent on the TO LINE Jack. When the ON HK button is engaged, the SF:FROM EQUIP Jack is terminated in 600 ohms.

MON — When this button is engaged, the SF:FROM EQUIP Jack is connected to the SF:TO LINE Jack. This allows monitor measurements to be made on the local sending unit, without interrupting the circuit, when the REC INTERFACE:FROM DROP/EQ button is engaged.

OFF HK & PULSE — When this button and the SEND INTERFACE: TWD LINE button are engaged, the tone output of the SF Level Control circuit is gated by the Pulse Generator output signal and sent on the SF:TO LINE Jack. If this button and the SEND INTERFACE:TWD DROP/EQ are engaged, no tone (OFF HOOK) appears at the SF:TO EQUIP Jack. When this button is engaged, the SF:FROM LINE Jack is terminated in 600 ohms.

d. SF LEVEL — This two digit thumbwheel switch, part of the ADJUST SEND SIGNAL controls, selects the output level of the SF tone to be sent. The level is in -dBm with reference to the sending impedance.

e. SF IMP — These three buttons select the sending impedance for the SF:TO EQUIP and SF:TO LINE Jacks. The receive impedance is always 600 ohms.

4.6.03 Circuit Connections

a. The four SF jacks are used to connect the Test Set to the SF circuit. To prevent service interruptions the REC INTERFACE and SF Supervision buttons should be set to provide monitoring on a bridging basis described in Section 4.6.04. The FROM LINE and TO EQUIP jacks are the receive side jacks or the +7 TLP jacks. The TO LINE and FROM EQUIP jacks are the transmit side or the -16 TLP jacks.

4.6.04 SF Monitoring

a. The T222C has the ability to monitor the send or receive side of the 4-wire circuit on a high impedance basis. Three related functions (supervision status determination, pulse measurements, level and frequency measurements) may be performed by the set in the monitoring mode with the same buttons engaged. The following buttons are operated:

ENGAGED
REC INTERFACE:SF
*REC INTERFACE:FROM LINE or FROM DROP/EQ
SF Supervision:TWD LINE:MON
SF Supervision:TWD EQUIP:MON

*When the REC INTERFACE:FROM LINE is engaged, the received signals will

be from the incoming or receiving side. When the FROM DROP/EQ button is engaged the received signals will be from the local equipment or the transmit side.

b. The supervision of either the transmit or receive side is determined by engaging the REC INTERFACE button for the desired direction and observing the REC ON HK Lamp. The supervision is indicated as follows:

Lamp	Supervision
ON	On Hook
OFF	Off Hook
PULSING	Pulsing

c. Pulse measurements for either the transmit or the receive side are also determined by the engaged FROM LINE or FROM DROP/EQ button. When pulsing is received, the Test Set displays the measured parameters selected by the Display Control buttons.

d. Frequency and level are automatically measured and displayed when the set identifies an SF tone as a valid On Hook signal. Since the T222C uses 600 ohms as the reference for level measurements, the following correction factors need to be applied to the displayed LEVEL measurement. If the nominal circuit impedance is 900 ohms, subtract 2 dB from the displayed level to obtain the level in dBm, 600 ohm. If the nominal circuit impedance is 1200 ohms, add 1 dB to the displayed level to obtain the level in dBm, 1200 ohms. These corrections apply ONLY to level measurements made in the monitoring mode.

4.6.05 Terminated SF Measurements

a. The Test Set makes terminated measurements into a 600 ohm impedance. Since service must be interrupted to make terminated measurements, the circuit should be idle.

1. To make terminated measurements on the receive side - from the line - the following buttons are operated:

ENGAGED

REC INTERFACE:SF
REC INTERFACE:FROM LINE
*SF Supervision:TWD EQ
**SF Supervision:TWD LINE
Set SF LEVEL (thumbwheel) to 24.

*If the local equipment requires Off Hook supervision, the OFF HK & PULSE button is engaged; if On Hook is required, the ON HK button is engaged. Normally the OFF HK & PULSE

button is engaged.

**If the transmit side requires a through connection, the MON button is engaged; if not, select either the ON HK or the OFF HK & PULSE for the transmit side supervision. Normally the OFF HK & PULSE button is engaged.

2. To make terminated measurements on the transmit side - from the local equipment - the following buttons are operated.

ENGAGED
REC INTERFACE:SF
REC INTERFACE:FROM DROP/EQ
*SF Supervision:TWD LINE
**SF Supervision:TWD EQ
SF LEVEL (thumbwheel) to 24.

*If the line requires Off Hook Supervision, the OFF HK & PULSE button is engaged; if On Hook is desired, ON HK button is engaged. Normally OFF HK & PULSE is engaged.

**If the receive side requires a through connection, the MON button is engaged; if not, either ON HK or OFF HK & PULSE is engaged. Normally OFF HK & PULSE is engaged.

b. After engaging the correct buttons for the desired direction of measurements, the operation is the same for either direction. The REC ON HK Lamp indicates the supervision or pulsing that is being received. When pulsing is received, the Test Set displays the measured parameters selected by the Display Control buttons.

c. When the Test Set is used in the terminating mode and the SF circuit is idle (On Hook), the Test Set automatically measures and displays the Frequency and Level of the incoming tone. If the nominal impedance of the SF circuit being measured is 900 ohms, the measurement error due to the 600 ohm termination is only -0.17 dB. For a 1200 ohm circuit the error is -.48 dB. Since the T222C measures and displays only to ±1 dB, the inaccuracy due to the unmatched impedances cannot be observed and the displayed 600 serves only to indicate the terminating impedance.

4.6.06 Sending SF

a. The Test Set may be connected into the SF circuit with one of three selectable impedances: 600, 900 or 1200 ohms. The transmit section is dc blocked and transformer coupled. Since service must be interrupted for pulsing, the circuit should be idle.

1. To pulse the local equipment or receive side of the circuit the following buttons are operated:

   ENGAGED

   SEND INTERFACE:SF
   SEND INTERFACE:TWD DROP/EQ
   SF Supervision:TWD EQUIP:OFF HK & PULSE
   *SF Supervision:TWD LINE
   SF LEVEL:Set to 1 dBm (-8 dBm0 pulsing level)
   SF IMP:(Set to correct impedance)

   *If the line requires On Hook supervision, engage the ON HK button. Normally OFF HK & PULSE is engaged.

2. To pulse the line or transmit side of the circuit the following buttons are operated:

   ENGAGED

   SEND INTERFACE:SF
   SEND INTERFACE:TWD LINE
   SF Supervision:TWD LINE:OFF HK & PULSE
   *SF Supervision:TWD EQUIP
   SF LEVEL:Set to 24 dBm (-8 dBm0 pulsing level)
   SF IMP:(Set to correct impedance)

   *If the local equipment requires On Hook supervision, engage the ON HK button. Normally OFF HK & PULSE is engaged.

b. After engaging the correct buttons for the desred direction of pulsing, the operation is the same for both directions. Pulsing is determined by the operation of the Pulse Generator controls.

4.7 E&M OPERATION

4.7.01 General -- The E&M Section of the Test Set provides circuits for both outpulsing and detection on the E and M leads. The Line (L) & Drop (D) lamps located to the left & right of the E&M Supervision controls are operated by the solid state high impedance E and M lead detectors. The outpulsing is done by solid state E lead (ground and open) or M lead (battery and ground) pulsers. The receiving is done with solid state terminating detectors. The ability to monitor an E&M circuit is also provided. The monitoring is accomplished by the high impedance E&M detectors, which also drive the Line and Drop lamps. The Test Set can also be used to pulse and measure the Type II and Type III E&M circuits with the same procedure for Type I operation.

4.7.02 Description of Controls -- This section covers the controls that are used for E&M operation. The controls that are unique to E&M operation are color coded blue.

a. REC INTERFACE — The following three buttons are used for E&M receiving.

1. E&M — This button is used for all types of E&M circuits. It selects the E&M detectors and connects their output to the Measuring Circuits so the requested data can be calculated and displayed.

2. FROM LINE — This button is used to select the line side detectors. When the button is engaged, the output of either the high impedance or the terminating E lead detector (determined by the position of the E&M:TWD DROP:MON Supervision button) is selected and connected to the Measuring Circuits by the E&M button.

3. FROM DROP/EQ — This button is used to select the drop side detectors. When engaged, the output of either the high impedance or the terminating M lead detector (determined by the position of the E&M:TWD LINE:MON Supervision button) is selected and connected to the Measuring Circuits.

b. SEND INTERFACE — The following three buttons are used to select the type and direction of E&M outpulsing.

1. E&M — This button, when engaged, connects the Pulse Generator output to the E&M Send Interface and Supervision Controls for pulsing the E lead or M lead pulsing circuits.

2. TWD LINE — This button, when engaged, connects the Pulse Generator output to the M lead pulser.

3. TWD DROP/EQ — This button, when engaged, connects the Pulse Generator to the E lead pulser.

c. E&M Supervision Controls -- The following six buttons, in conjunction with the SEND INTERFACE controls, determine the supervision presented to the E&M:LINE and DROP jacks.

1. The three TWD DROP buttons determine the supervision for the E&M:DROP jack as follows:

ON HK — When engaged, the Test Set sends an On Hook (open) on the tip (E lead) of the E&M:DROP jack. The tip of the E&M:LINE jack is terminated and the "L" (line) lamp displays the status of the line.

MON — When engaged, the E lead is connected through the Test Set - the tip of the E&M:LINE jack is connected to the tip of the E&M:DROP jack. The high impedance E lead detector drives the LINE lamp and also drives the measuring circuits if the REC INTERFACE:FROM DROP/EQ button is engaged.

OFF HK & PULSE — When engaged, the E lead from the E&M:LINE jack is terminated and an Off Hook (ground) is sent on the E lead of the E&M:DROP jack by the E lead pulser. If the SEND INTERFACE:TWD DROP/EQ button is engaged, the E lead pulser is controlled by the Pulse Generator output.

2. The three TWD LINE buttons determine the supervision for the E&M:LINE jack as follows:

ON HK — When engaged, the Test Set sends an On Hook (ground) on the ring (M lead) of the E&M:LINE jack. The ring of the E&M:DROP jack is terminated and the "D" (drop) lamp displays the supervision from the drop.

MON — When engaged, the M lead is connected through the Test Set - the ring of the E&M:LINE jack is connected to the ring of the E&M:DROP jack. The high impedance M lead detector drives the DROP lamp and also drives the measuring circuits if the REC INTERFACE:FROM LINE button is engaged.

OFF HK & PULSE — When engaged, the M lead from the E&M:DROP jack is terminated and an Off Hook (battery) is sent on the M lead of the E&M:LINE jack by the M lead pulser. If the SEND INTERFACE:TWD LINE button is engaged, the M lead pulser is controlled by the Pulse Generator output.

4.7.03 Circuit Connections

a. The two E&M jacks are used to connect the Test Set to the E&M circuit. To prevent service interruptions the REC INTERFACE and E&M Supervision buttons should be set to provide monitoring on a bridging basis as described in Section 4.4.04 before patching to the circuit. The LINE jack is connected to the line side of the E&M circuit; the M lead pulser is on the ring of this jack and the E lead detectors are on the tip. The DROP jack is connected to the drop side of the E&M circuit; the E lead pulser is on the tip of this jack and the M lead detectors are on the ring.

4.7.04 E&M Monitoring

a. The Test Set has the ability to monitor the E lead and M lead on a high impedance (bridging) basis without affecting the performance of the circuit and without taking the circuit out of service. The following buttons are operated:

ENGAGED

REC INTERFACE:E&M
E&M Supervision:TWD LINE:MON
E&M Supervision:TWD DROP:MON

b. The status of the E lead and M lead is indicated by the "L" and "D" lamps. Pulsing on either lead is measured and displayed by engaging the REC INTERFACE:FROM DROP/EQ or FROM LINE button and the desired Display Controls.

4.7.05 Terminated E&M Measurements

a. The Test Set makes terminated E&M pulse measurements into a 470 ohm impedance. Since service must be interrupted to make terminated measurements, the circuit should be idle.

1. To make terminated measurements on the E lead, from the line, the following buttons are operated:

ENGAGED

REC INTERFACE:E&M
REC INTERFACE:FROM LINE
*E&M Supervision:TWD DROP

*Either the ON HK or the OFF HK & PULSE button is engaged depending on supervision to be sent toward the Drop. Normally the OFF HK & PULSE button is engaged.

2. To make terminated measurements on the M lead, from the drop, the following buttons are operated:

ENGAGED

REC INTERFACE:E&M
REC INTERFACE:FROM DROP/EQ
*E&M Supervision:TWD LINE

*Either the ON HK or the OFF HK & PULSE button is engaged depending on supervision to be sent toward

the line. Normally the OFF HK & PULSE button is engaged.

b. After engaging the correct buttons for the desired measurement direction, the operation is the same for either direction. The REC ON HK lamp indicates the supervision or pulsing that is being received. When pulsing is received, the Test Set displays the measured parameters selected by the Display Control buttons.

4.7.06 Pulsing E&M

a. When pulsing E&M, the circuit has to be broken between the Line and Drop. It is recommended that the monitor test above be done to determine that the circuit is idle before pulsing tests are performed.

1. FOR PULSING THE LINE:

The following buttons are operated:

ENGAGED

SEND INTERFACE:E&M
SEND INTERFACE:TWD LINE
E&M Supervision:TWD LINE, OFF HK & PULSE

NOTE: Supervision toward the Drop can be accomplished by engaging the appropriate button under the E&M Supervision TWD DROP. If the Line is to supervise the Drop the TWD DROP:MON button should be engaged. Otherwise the OFF HK & PULSE button should be engaged.

2. For pulsing the drop:

The following buttons are operated:

ENGAGED

SEND INTERFACE:E&M
SEND INTERFACE:TWD DROP/EQ
E&M Supervision:TWD DROP, OFF HK & PULSE

NOTE: Supervision toward the Line can be accomplished by engaging the appropriate E&M Supervision buttons under the TWD LINE.

b. Now patch the Test Set to the circuit using the E&M LINE and DROP Jacks. The desired pulsing may now be performed by operating the appropriate ADJUST SEND SIGNAL and PULSING Controls.

4.8 DX OPERATION

4.8.01 General -- The DX Section interfaces the DX signaling system at the A & B Leads or the 2W tip and ring. The ability to monitor on an in-service or out-of-service basis is provided. In a DX signaling system the Line side is defined as the more distant DX unit and the Equipment side is the closer DX unit. This is the terminology in this operational section.

4.8.02 Description of Controls -- This section covers the controls that are used in DX operation. Those push buttons that are unique to DX operation are identified by a cream colored button.

a. REC INTERFACE — The following four buttons are used for DX operation.

1. DX — This button, when engaged, connects the output of either the high impedance DX detector or the low impedance DX receiver to the T222C measuring circuits.

2. STATUS — This button is used to select the A/B Detector and the A/B Lamp when the status of the DX loop is to be determined.

3. FROM LINE and FROM DROP/EQ — These two buttons select the direction for receiving or Status indication; either toward the line or toward the equipment.

b. SEND INTERFACE — The following four buttons are used in the DX mode of operation.

1. DX — This button, when engaged, connects the output of the Pulse Generator to the DX pulser.

2. ADD RES — This button, when engaged, adds the amount of the ADD LOOP RESISTANCE buttons to the output of the DX Pulser. When switching from the EQUIP side to LINE side, only the ADD RES button needs to be used instead of changing all the Loop Resistance buttons.

3. TWD LINE & TWD DROP/EQ — These two buttons select the direction of pulsing. The TWD LINE, when engaged, will present the pulsing on the A lead of the DX LINE jack. When the TWD DROP/EQ button is engaged, the pulsing is presented to the A lead of the DX EQUIP jack.

NOTE: When the REC INTERFACE:DX button is engaged, the REC INTERFACE direction controls override those of the SEND INTERFACE. For example; if the REC INTERFACE: FROM LINE button is engaged, the output of the DX Pulser is connected toward the equipment regardless of the SEND INTERFACE:TWD DROP/EQ and TWD LINE button positions.

c. DX Supervision Controls -- The following five buttons, determine the supervision and operation for the DX functions.

1. MON — This button connects the DX:EQUIP and LINE jacks through the Test Set and connects the high impedance monitor to the circuit. When connecting into the DX circuit of unknown supervision state, the DX:MON button should be engaged.

2. PULSE & STATUS — This button breaks the DX Loop and terminates each lead. This condition is used for pulsing, status determination or terminated DX receiving.

3. A/B:REV/NORM — This button reverses the A & B Lead orientation. The released position is the normal orientation A lead on tip and B lead on ring. The engaged position is the reverse condition.

4. OFF HK/ON HK — This button is used in conjunction with the DX MON button. This selects one of two high impedance DX Monitor Receivers in the set. The released position or ON HK is used to monitor the DX circuit when the receiving end is On Hook. The engaged position or OFF HK is used to monitor when the receiving end is Off Hook.

5. REV SUPV:OFF HK/ON HK — This button selects the reverse supervision when operating in either the DX REC terminating or DX Pulsing modes. The released position (ON HK) places an ON HOOK (Ground) in reverse direction from the sending or receiving direction. The engaged position places an Off Hook or battery in the reverse direction.

4.8.03 Status Determination

a. Operation -- Two ways are available for determining the status of a DX Circuit. The first way, assumptions are made and the second way the circuit is broken and terminated. To determine the status of the circuit without interrupting it; is to assume that the A lead is on the tip and B lead is on the ring. Operate the following buttons:

ENGAGED	RELEASED
REC INTERFACE:DX	DX Supervision:OFF HK/ON HK (ON HK)
DX Supervision:MON	DX Supervision:A/B (NORM)

b. Plug the circuit into the DX:EQUIP and LINE jacks; the Equipment side to the EQUIP jack and the Line side to the Line jack. If the circuit is idle, the DX ON HOOK lamp will be lighted. If the DX ON HOOK lamp does not light, an A/B reverse check should be made. Engage the DX A/B REV button. If the DX:ON HOOK lamp lights then the circuit is idle but the A & B leads were reversed from normal. If the lamp does not light, then either the circuit is busy or a fault exists.

c. The second way of status determination requires that the circuit be broken; therefore, the circuit should be out of service to prevent the interruption of calls. Operate the following buttons:

ENGAGE	RELEASED
REC INTERFACE:DX	DX Supervision:A/B(NORM)
DX Supervision:PULSE & STATUS	DX Supervision:REV SUPV

d. Plug the circuit into the DX:EQUIP and LINE jacks as previously described.

e. To check the Equip side, engage the REC INTERFACE:FROM DROP/EQ and STATUS buttons; STATUS button is held in for the duration of this test. Observe the DX:ON HOOK and A/B lamps. If the lamp is lighted, the A/B leads are in the correct orientation. If the lamp is not lighted, then engage the A/B REV button; the lamp should now be lighted. When the correct orientation of the A/B leads is achieved, (lighted A/B lamp), then observe the DX:ON HK lamp. If the DX:ON HOOK lamp is lighted, the Equip side is On Hook. To observe the Line side, engage the REC INTERFACE:FROM LINE button and observe the DX:ON HOOK lamp. If it is lighted, then the Line side is On Hook. If while observing either the Line or Equip side the DX:ON HOOK lamp did not light, then that particular direction was sending an Off Hook.

4.8.04 High Impedance Monitoring

a. The ability to monitor pulsing on a high impedance basis is available in the T222C. There are two conditions at the receiving end that can exist on the DX circuit; either On Hook or Off Hook. To monitor with the receiving end On Hook the following

buttons are operated:

ENGAGED	RELEASED
REC INTERFACE:DX DX Supervision:MON	DX Supervision:OFF HK/ON HK (ON HK)

NOTE: The A/B REV button should be in the position for the correct orientation of the leads.

b. The DX:ON HOOK lamp indicates the supervision and pulsing of the circuit. The Display mode may now be selected for the information desired. If the receiving end is Off Hook, then engage the DX Supervision:OFF HK/ON HK button (OFF HK). The DX:ON HOOK lamp indicates the supervision or pulsing of the circuit and the display shows the pulses in response to the engaged Display Controls.

4.8.05 Terminated Receiving

a. The DX circuit may be terminated and receiving from either the Line or the Equip side may be performed. To receive terminated the following buttons are operated:

ENGAGED	RELEASED
REC INTERFACE:DX DX Supervision:PULSE & STATUS	SEND INTERFACE:DX

NOTE: The A/B button should be in the position for correct orientation of the A/B leads. The DX Supervision:REV SUPV button should be set to the desired position; either ON HK, released, or OFF HK, engaged.

4.8.06 DX Pulsing

a. After a status determination test has been completed, the DX Circuit can be pulsed. The following buttons have to be operated.

ENGAGED	RELEASED
SEND INTERFACE:DX DX Supervision:PULSE & STATUS	REC INTERFACE:DX

NOTE: The DX Supervision:A/B and REV SUPV buttons should be set to the appropriate positions. The ADD LOOP RESISTANCE buttons should be set to the positions to make up the correct line resistance in the DX circuit.

b. Plug the circuit under test into the DX:EQUIP and LINE jacks. To pulse the Line side; remove the line resistance by releasing the ADD RES button, engage the SEND INTERFACE:TWD LINE button and operate the Send Controls for the desired pulsing. To pulse the Equip side; add the line resistance, by engaging the ADD RES button, engage the SEND INTERFACE:TWD DROP/EQ button and operate the Send Controls for the desired pulsing.

5.0 OPERATIONAL CHECKS

5.1 General

5.1.01 This section will cover the checks that may be made by the operator, using only a patch cord, to verify the operation of the Test Set. The individual sections are designed to check various portions of the Test Set to isolate problems for repair purposes.

5.1.02 Tolerance, where not specified, is ±2 count in the least significant digit.

5.2 Initial Conditions

5.2.01 The following procedure establishes the correct control positions so that the Test Set will "come up" in a known operating mode when power is applied.

a. Engage the following buttons:

DISPLAY CONTROL:MODE:MEAS:REC
REC INTERFACE:LOOP
SEND CONTROL:ON HK (Pulse Generator)
INTERDIGIT TIME:400+200+100

b. Set the POWER switch to the ON position. The LINE, REC ON HK, and the DX:ON HOOK lamps should be lighted and the word READY displayed.

c. If the PULSE and INTERDIGIT lamps are flashing, push the "*" key momentarily to stop pulsing.

d. If the word READY is not displayed, push the DISPLAY CONTROL: MODE, CLEAR button.

e. If the MANUAL lamp is not lit, press the "*" key for 2 seconds.

5.3 Pulse Generator and Display Checks

5.3.01 The Pulse Generator and the Display sections have to be checked together. This section is divided into various tests. Test A will verify the basic operation of the Pulse Generator. Test B will check the Pulse Generator, Measurements, and Display Sections for their Speed and % Break functions. Test C will check the Pulse Generator and Display for the proper keyboard operation and Dialed Number Display function. Test D will check the rest of the Display functions.

TEST A	
Action	Result
1. Engage the SEND CONTROL: DIGIT button.	

TEST A Continued

Action	Result
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Press "0" key of Keyboard	The Pulse Lamp should pulse 10 times. The Interdigit Lamp should light after end of pulsing for a period of 700 ms and then go off.
4. Press # Keyboard key	The Set should repeat pulsing 10 pulses with the interdigit interval.
5. Press * Keyboard key momentarily	Pulsing stops.

TEST B

Action	Result
1. Set the following buttons as indicated. Engaged — DISPLAY CONTROL: % BRK PPS MEAS:PULSE GEN UPDATE SEND CONTROL: TRAIN Released — DISPLAY CONTROL: COUNT PULSES DIALED NUMBER 2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	

Action	Result
3. Press "0" Keyboard digit	REC ON HK lamp should pulse and Display should read 60.0 %BK 12.0 PPS ✓
4. Set the ADJUST SEND SIGNAL: SPEED to 22.	Display: 60.0 %BK 22.0 PPS ✓
5. Set the ADJUST SEND SIGNAL: SPEED to 02.	Display: 60.0 %BK 02.0 PPS ✓
6. Set the ADJUST SEND SIGNAL: SPEED thumbwheel to each position from 02 to 09.	The Display should read the same PPS as the setting of the SPEED thumbwheel. ✓
7. Set the ADJUST SEND SIGNAL: SPEED thumbwheel to 05 and adjust the % BREAK thumbwheel to each position from 60 to 69.	The %BK portion of the Display should follow the setting of the % BREAK thumbwheel. ✓
8. Adjust the % BREAK thumbwheel to each position from 20 to 90 by 10's.	The %BK portion of the display should follow the setting of the % BREAK thumbwheel. ✓
9. Press * Keyboard key momentarily.	Pulsing stops. REC ON HK OFF ✓

TEST C	
Action	Result
1. Engage the following buttons: DISPLAY CONTROL: DIALED NUMBER MEAS:PULSE GEN SEND CONTROL: DIGIT	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Press "1" Keyboard digit	Display: 1 NMBR ✓

Action	Result
4. Press in succession keyboard "2" thru "0"	Display: 1234567890 NMBR
5. Press DISPLAY CONTROL:CLEAR button.	Display: READY

TEST D	
Action	Result
1. Set the following buttons as indicated. Engaged -- DISPLAY CONTROL: WIDTH PERIOD MEAS:PULSE GEN UPDATE SEND CONTROL: DIGIT Released -- DISPLAY CONTROL: COUNT PULSES DIALED NUMBER	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Press "0" Keyboard digit	Display: 50.0 WID 83.3 PER
4. Engage the DISPLAY CONTROL: AVG button.	
5. Press "9" Keyboard digit	Display: 50.0 WID 83.3 PER AV*
6. Engage the DISPLAY CONTROL: COUNT PULSES button and push the DISPLAY CONTROL: CLEAR button.	Display: READY

TEST D Continued

Action	Result
7. Press "0" Keyboard digit	Display: 010 PULSES
8. Release the DISPLAY CONTROL: COUNT PULSES button and push the DISPLAY CONTROL: CLEAR button.	Display: READY
9. Press "0" Keyboard digit	Display: 50.0 WID 83.3 PER AV9
10. Push the DISPLAY CONTROL: PULSE DATA button.	Display: 50.0 WID 83.3 PER P#1
11. Push the DISPLAY CONTROL: CLEAR button.	Display: READY

5.4 LOOP Checks

5.4.01 This section will cover the tests which can be performed to verify the operation of the Loop Interface Send and Receive sections. Test A will verify the Loop Receivers and Loop Contact Closure Pulser. Test B will check the Battery and Ground Pulser.

TEST A

Action	Result
1. Set the following buttons as indicated. Engaged -- DISPLAY CONTROL: % BRK PPS MEAS:REC AVG SEND CONTROL: DIGIT ADD LOOP RESISTANCE: 400 800 LEAK COND: OUT (IN) "PRESSED" "A" SEND INTERFACE: LOOP REC INTERFACE: LOOP	

Action	Result
Released -- DISPLAY CONTROL: COUNT PULSES DIALED NUMBER SEND INTERFACE: B&G/NORM REC INTERFACE: "A" RLY/DIRECT	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Push the DISPLAY CONTROL: CLEAR button.	Display: READY
4. Patch the LOOP:SEND jack to the LOOP:TERM REC jack.	REC ON HK Lamp is no longer lighted.
5. Press "0" Keyboard digit	Display: 60.0 %BK 12.0 PPS AV9
6. Release the LEAK COND: OUT button and engage the REC INTERFACE:"A"RLY/DIRECT button.	
7. Press "0" and then the "#" Keyboard keys.	60.9% Display: 60.0 %BK ±.5%BK 12 PPS AV9
8. Press "*" Keyboard key.	Pulsing stops.
9. Move the patch cord from the LOOP:SEND jack to the LOOP: S/R jack. MEAS PULSE GEN	
10. Push the DISPLAY CONTROL: CLEAR button.	Display: READY
11. Press "0" and then the "#" Keyboard keys.	60.9 % Display: 60.0 %BK ±.5% 12 PPS AV9
12. Press "*" Keyboard key.	Pulsing stops.

TEST B	
Action	Result
1. Set the following buttons as indicated.	

Action	Result
Engaged -- DISPLAY CONTROL: %BRK PPS MEAS:REC AVG SEND CONTROL: DIGIT ADD LOOP RESISTANCE: 3.2k 400 200 LEAK COND: OUT SEND INTERFACE: B&G/NORM LOOP REC INTERFACE: LOOP Released -- DISPLAY CONTROL: COUNT PULSES DIALED NUMBER REC INTERFACE: "A" RLY/DIRECT	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Push the DISPLAY CONTROL: CLEAR button.	Display: READY
4. Press "0" and then the "#" Keyboard keys.	Display: 60.0 %BK 12.0 PPS AV9
5. Press "*" Keyboard key.	Pulsing stops.

5.5 E&M Checks

5.5.01 This section will cover the tests which may be performed to verify the operation of the E&M Send and Receive functions.

TEST A	
Action	Result
1. Set the following buttons as indicated.	

Action	Result
Engaged -- DISPLAY CONTROL: % BRK PPS MEAS:REC UPDATE SEND CONTROL: DIGIT SEND INTERFACE: E&M TWD DROP/EQ E&M Supervision: TWD DROP:OFF HK & PULSE TWD LINE:ON HK REC INTERFACE: E&M FROM LINE	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Patch the E&M:LINE jack to the E&M:DROP jack.	The LINE lamp and REC ON HOOK lamp go out.
4. Press "0" and then the "#" Keyboard keys.	DISPLAY: 60.0 %BK 12.0 PPS The LINE and REC ON HK lamps pulse.
5. Press "*" Keyboard key.	Pulsing stops.
6. Engage the E&M:TWD DROP: ON HK supervision button.	The REC ON HK and LINE lamps light.
7. Engage the following buttons: SEND INTERFACE: TWD LINE E&M:TWD LINE:OFF HK & PULSE REC INTERFACE: FROM DROP/EQ	REC ON HK LAMP GO OUT.
8. Press "0" and then the "#" Keyboard keys.	DISPLAY: 59.9 %BK 12.0 PPS REC ON HK and DROP lamps pulse.
9. Engage the E&M:TWD LINE: ON HK Supervision button.	DROP & REC ON HK lamps light.

10. Press "*" Keyboard key.	Pulsing stops.

5.6 SF Checks

5.6.01 The following test will allow the operator to check the SF Send and Receive sections for pulsing operation and the measurement of frequency and level.

TEST A	
Action	Result
1. Set the following buttons as indicated: Engaged -- DISPLAY CONTROL: % BRK PPS MEAS:REC AVG SEND CONTROL:DIGIT SF IMP:900 SF FREQ:2600 SEND INTERFACE: SF TWD DROP/EQ SF Supervision: TWD EQUIP:OFF HK & PULSE TWD LINE:OFF HK & PULSE REC INTERFACE: SF FROM LINE Released -- DISPLAY CONTROL: COUNT PULSES DIALED NUMBER	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED -- 12 % BREAK -- 60 SF LEVEL -- 13	
3. Patch the SF:TO EQUIP jack to the SF:FROM LINE jack.	
4. Press "0" and then the "#" Keyboard keys.	DISPLAY: 60.1 ±.5 %BK 12.0 PPS AV9

TEST A Continued

Action	Result
5. Press "*" Keyboard key.	Pulsing stops.
6. Engage the supervison SF:TWD EQUIP:ON HK button.	DISPLAY: FREQ = 2600 Hz; ±5 Hz LEVEL = -13 dBm (600) ±1 dB
7. Engage the SEND INTERFACE: TWD LINE button.	DISPLAY: FREQ = 2600 Hz; ±5 Hz LEVEL = -20 dBm (600) ±1 dB
8. Engage the REC INTERFACE: FROM DROP/EQ button.	REC ON HK lamp goes out.
9. Patch the SF:TO LINE jack to the SF:FROM EQUIP jack.	
10. Press "0" and then the "#" Keyboard keys.	60.1 × DISPLAY: 60.1 ±.5 %BK 12.0 PPS AV9
11. Press "*" Keyboard key.	Pulsing stops.
12. Engage the supervision SF:TWD LINE:ON HK button.	DISPLAY: FREQ = 2600 Hz; ±5 Hz LEVEL = -13 dBm (600) ±1 dB

5.7 DX Checks

5.7.01 The following test will allow the operator to verify the operation of the DX Send and Receive sections.

TEST A

Action	Result
1. Set the following buttons as indicated. Engaged -- DISPLAY CONTROL: % BRK PPS MEAS:REC AVG SEND CONTROL: DIGIT ADD LOOP RESISTANCE: 1.6k 400 SEND INTERFACE: DX	

Action	Result
TWD LINE ADD RES REC INTERFACE: DX FROM DROP/EQ DX SUPERVISION PULSE & STATUS Released -- DISPLAY CONTROL: COUNT PULSES DIALED NUMBER	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED -- 12 % BREAK -- 60	
3. Patch the DX:LINE jack to the DX:EQUIP jack.	REC ON HK Lamp will go out.
4. Press "0" and then the "#" Keyboard keys.	DISPLAY: 60.0 %BRK 12.0 PPS AV9 DX:ON HOOK and REC ON HK Lamps are pulsing.
5. Press "*" Keyboard key.	Pulsing stops.
6. Engage the SEND INTERFACE: SF button.	
7. Engage the DX:REV SUPV button.	DX:ON HOOK and REC ON HK Lamps are not illuminated.
8. Release the DX:REV SUPV button.	DX:ON HOOK and REC ON HK Lamps are illuminated.
9. Press the REC INTERFACE: STATUS button.	A/B Lamp illuminates while the STATUS button is pressed.

5.8 Dialed Number Storage Checks

5.8.01 The following test will allow the operator to verify the operation of the Dialed Number Storage Section.

Action	Result
1. Set the following buttons as indicated. Engaged -- DISPLAY CONTROL: DIALED NUMBER MEAS:PULSE GEN INTERDIGIT TIME:400+200+100 SEND CONTROL:DIGIT	
2. Set the ADJUST SEND SIGNAL controls as follows: SPEED — 12 % BREAK — 60	
3. Press the "*" key for 2 seconds.	Store lamp lights, Manual lamp turns off.
4. Enter the following digits: 1234567890123456	
5. Press the "#" (send) key.	DISPLAY: 1234567890123456
6. Press the PULSE DATA button.	DISPLAY: I.D. TIME = 700 msec ±3msec I.D. #1
7. Repeat step (6) 15 times.	
8. Press the CLEAR key.	
9. Press "*" momentarily.	
10. Enter the following digits: 123	
11. Press the "#" key.	DISPLAY: 123

6.0 CIRCUIT DESCRIPTION

6.1 General

6.1.01 The circuit functions for the Model T222C Signaling Test Set are described using a Functional Block Diagram figure 6-1 and overall Simplified Schematic Diagrams figure 6-3a thru figure 6-8. The detailed schematic diagrams and P.C. Assemblies in section 8.0 are needed for more detailed circuit tracing and for component location respectively. All drawings are provided with an "A" number code for rapid cross referencing.

6.2 Outpulsing Circuits

6.2.01 The Rate-% Break (pulse) Generator, A21, and related circuit assemblies A29 and A30 are controlled by inputs from the keyboard (dial), the SPEED and % BREAK thumbwheels and the SEND CONTROL push buttons. Two LED indicators, PULSE and INTERDIGIT, provide a visible indication of the pulsing mode of the pulse generator.

6.2.02 The Keyboard assembly (part of A15) converts the digits, entered from the keyboard into a two-of-seven output code. Located on this assembly are the PULSE, INTERDIGIT, MANUAL and STORE LED's as well as the drivers for both the MANUAL and STORE LED's. Switching diodes CR1 through CR24, figure 8-21, are used to diode-encode the keyboard output into a two-of-seven code used by the Keyboard Decoder-Store-Control A30.

6.2.03 The Keyboard Decoder-Store-Control (A30) accepts inputs from A15. It handles digit storage in either the MANUAL mode or the STORE mode and provides clock and timing for the send INTERDIGIT TIME.

U1 is a keyboard encoder circuit that accepts the two-of-seven code as well as a 2560 Hz clock input and provides debounce and a BDC output for the number entered. U3C and U3B decode the * and # keys and provide outputs that control the MANUAL or STORE mode selection by means of U4A, U4B and U5A. U6 is a latch which holds the numeric key entry whenever a stobe pulse is received from U1. It presents the entry to U7 which is a quad two-to-one multiplexer. The output of U7 to down counter U8 is data from U6 in the MANUAL mode and data read from RAM U10 in the STORE mode. U8 is advanced by the M-B signal from the Rate-% Break Generator, A21. When zero count is reached, U5B is reset starting the interdigit counter U13 and signaling ID to the Rate-% Break board as QIDT. U14 and U5 are level shifters which match logic levels on A30 to those on A21. In the STORE mode, as digits are entered they are stored in U10. Counter U12A and reference counter U12B are advanced by a clock pulse from U4D-C9 which is the strobe pulse with a short delay added. After digits have been entered and the send key (#) is pressed, stored digits are sequentially read from RAM and input to U8 via U7. After each digit has been pulsed out, U12A advances while U12B holds the reference

count (which is the number of digits previously entered). When U12A output equals U12B, comparator U11 resets U12A and generates a reset to A21. U18 and U19 provide a divide by 390 for the 1 MHz clock. This 2560 Hz output clocks U13, the interdigit counter.

6.2.04 INTERDIGIT TIME Select (A29) - This assembly accepts a front panel input for interdigital time selection and provides a reset pulse to U13 and assembly A30 when the proper count for the selected ID time has been reached by U13.

6.2.05 Rate-% Break Generator (A21) - The Rate-% Break Generator accepts BCD inputs from the speed thumbwheel switch and decimal inputs from the % Break Switch. It then generates a Make-Break signal at the speed and duration selected by the user. Also contained on this board is the start/stop logic used with A30.

The 1 MHz clock is input to cascaded BCD rate multipliers U3 and U4 where it is multiplied by .00 thru .29 in .01 steps. The output is further divided by U5 and U6 and the output of U6 is a pulse train with speed selectable from 0 thru 29 pulses per second. U7 and U8 are decade counters with decoded 1 of 10 outputs. The selected output are gated by U13 to control R-S flip flop U12B the output of which is of the selected duty cycle. U9 thru U12 form a run/stop control. U12A is clocked by the delayed KYB strobe (KYB on A30) and its output (or that of U10A-U9C as a result of the repeat key being pressed) sets U10B. $\bar{Q}$ on U10B, together with U9, generates an L.C.C. (load count clock) pulse which loads the down counter (U8) on A30. At this point, control is carried on by A30 until the next interdigit time or until stop (*) is momentarily pressed.

6.2.06 SEND CONTROL (A8) - Four interlocking push buttons with lock-out action are used to select the method of operation of the Pulse Generator (A21) i.e. TRAIN, DIGIT, ON HK, OFF HK. Section 3.3 describes the Pulse Generator Controls.

6.3 Self Scan * Display

6.3.01 DISPLAY CONTROL Switching (A10) - This assembly interfaces front panel control of display data to both the data input control and CPU assemblies. In addition, U1 and U2 form a validation circuit used for rejecting spurious pulses in the dialed number display mode. Also located on this assembly is the driver (Q1, 2) for the receive-on-hook indicator LED.

6.3.02 Interrupt Timer & Self Scan Interface (A23) - This assembly contains circuits which allow the Self Scan * display to place a hold on the CPU and perform a direct memory access (DMA) on the CPU memory. Also included on this assembly is the interrupt timer which generates a CPU interrupt signal from the master clock. Among other things, the interrupt routine forces the CPU to perform an A/D conversion and frequency display update.

* Burroughs Trademark

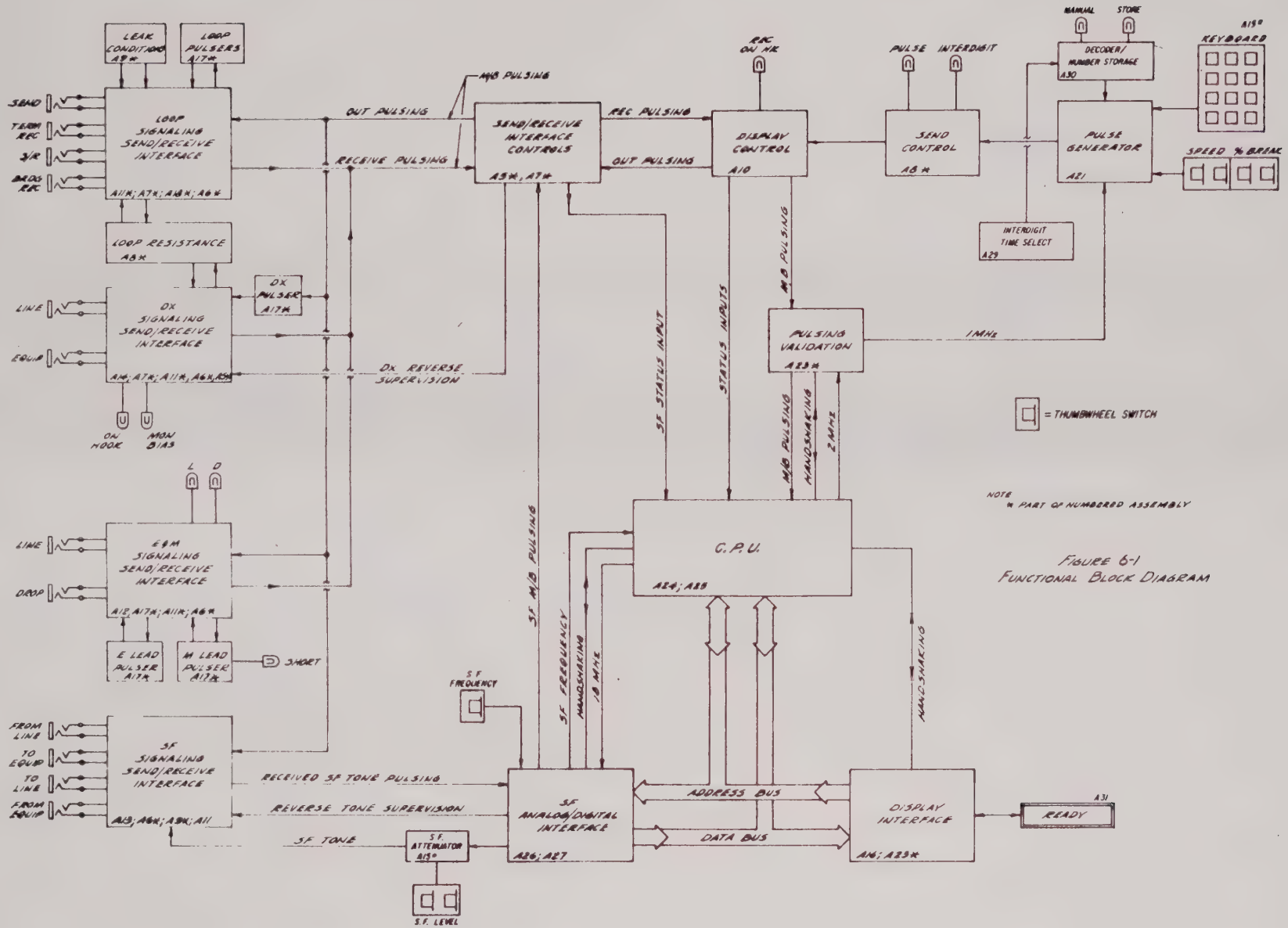


FIGURE 6-1
FUNCTIONAL BLOCK DIAGRAM

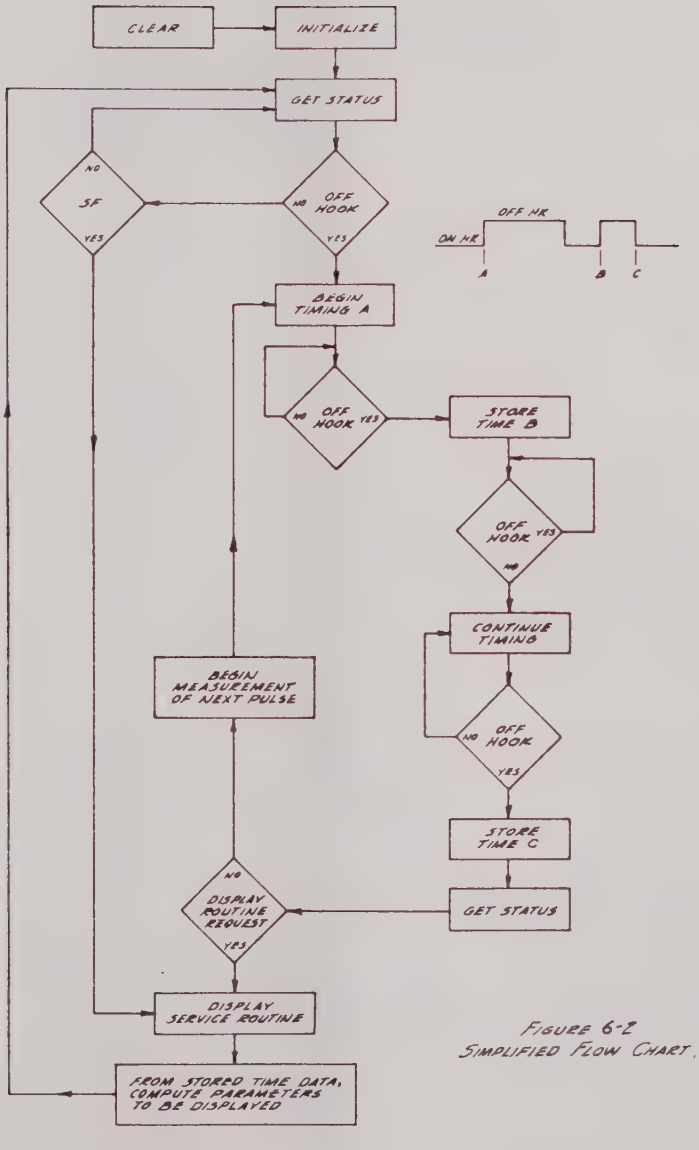
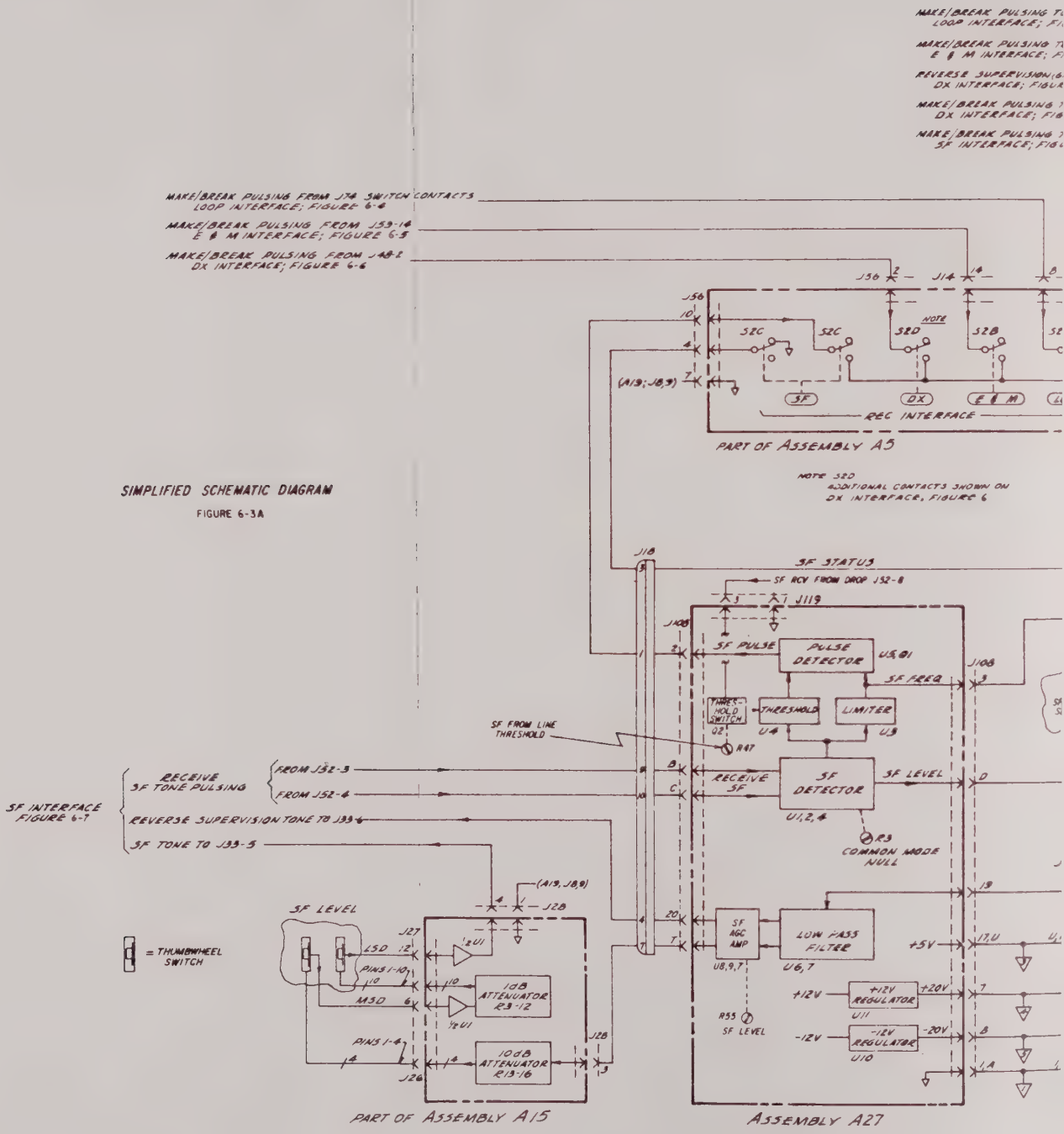


FIGURE 6-2
SIMPLIFIED FLOW CHART.


MAKE/BREAK PULSING FROM J74 SWITCH CONTACTS
LOOP INTERFACE; FIGURE 6-4
MAKE/BREAK PULSING FROM J53-14
E & M INTERFACE; FIGURE 6-5
MAKE/BREAK PULSING FROM J48-2
DX INTERFACE; FIGURE 6-6
J56
J14
S2C
S2D
S2B
NOTE
(A19; J8,9)
SF
DX
E & M
REC INTERFACE
PART OF ASSEMBLY A5
NOTE S2D
ADDITIONAL CONTACTS SHOWN ON
DX INTERFACE, FIGURE 6
SIMPLIFIED SCHEMATIC DIAGRAM
FIGURE 6-3A
J118
SF STATUS
SF RCV FROM DROP J52-8
J119
J108
SF PULSE
PULSE DETECTOR
U5,6,7
SF FREQ
THRES-HOLD SWITCH
THRESHOLD
LIMITER
U2
U4
U3
SF FROM LINE THRESHOLD
R47
RECEIVE SF TONE PULSING
FROM J52-3
FROM J52-4
RECEIVE SF
SF DETECTOR
U1,2,4
SF LEVEL
SF INTERFACE FIGURE 6-7
REVERSE SUPERVISION TONE TO J33-6
SF TONE TO J33-5
R3
COMMON MODE NULL
(A19, J8,9)
J28
SF LEVEL
J27
LSD
MSD
PINS 1-10
10dB ATTENUATOR R23-12
PINS 1-4
10dB ATTENUATOR R13-16
½ U1
= THUMBWHEEL SWITCH
SF AGC AMP
U8,9,7
LOW PASS FILTER
U6,7
+5V
+12V REGULATOR
U11
+20V
-12V REGULATOR
U10
-20V
R55
SF LEVEL
PART OF ASSEMBLY A15
ASSEMBLY A27

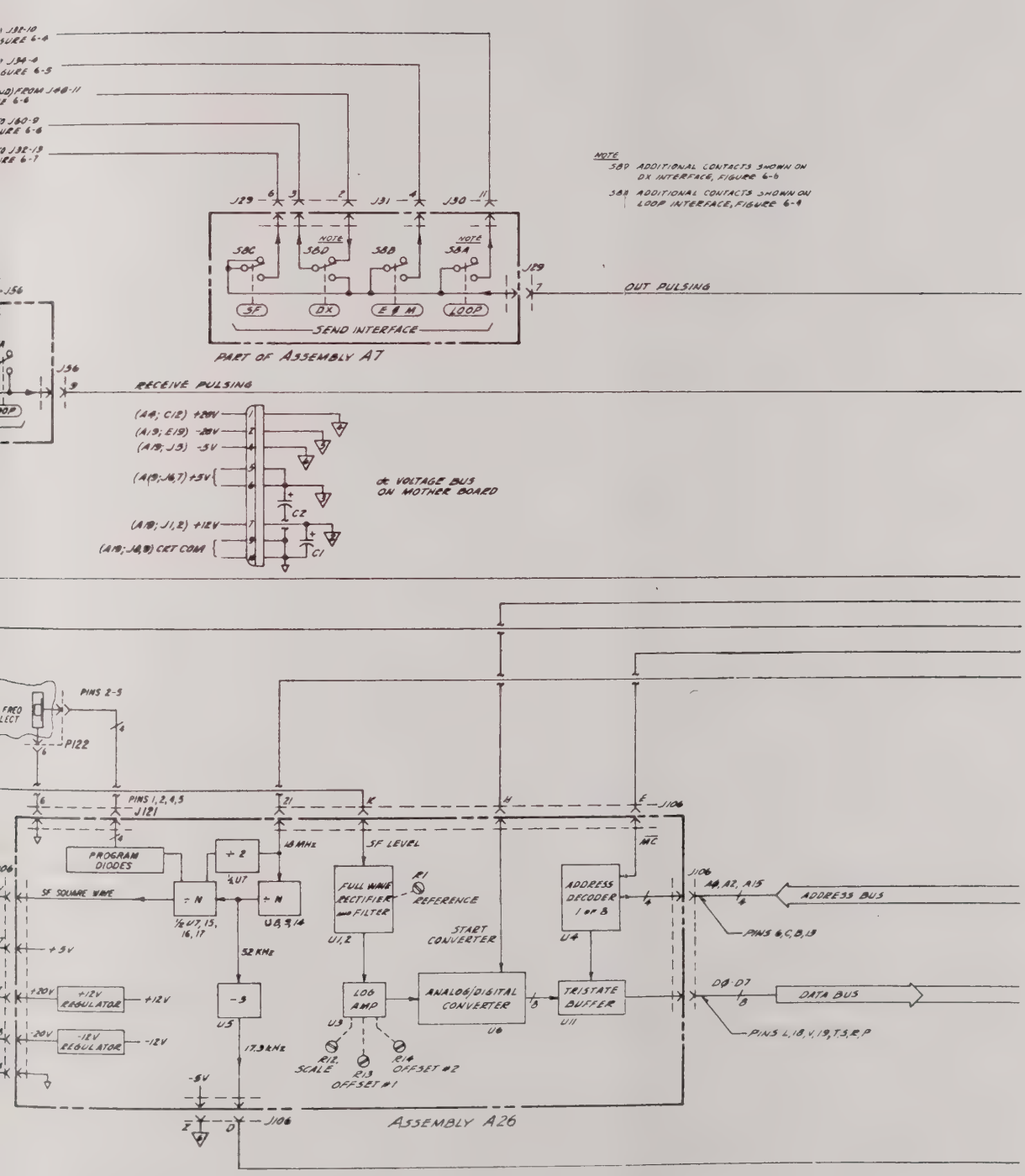


FIGURE 6-3A
Simplified Schematic

U12 thru U15 and parts of U7 and U8 form a divider chain which generates an interrupt every 320 ms. Also generated is a 1 MHz clock buffered and level shifted by Q1. This clock feeds the IDT clock circuit and the keyboard Store-Decoder assembly; it also feeds the Rate-% Break Generator board. U11, U16 and U7B form a debounce circuit which provides pulse validation for the input Make-Break signal. It will require that an input transition be stable for 8-10 ms. before changing its output. This circuit also disables the interrupt flip flop U15A to prevent an interrupt in the presence of an off hook (make). The Self Scan interface generates addresses in the range of 1C00H 1CFFH. The output update (Self Scan *) signal causes a hold to be generated by U3A. The CPU will return a hold acknowledge. At this point, the CPU address and data bus are tristated and U10, U2, U1 generate a RAM address between 1C00H - 1CFFH. The Self Scan * reads the data at this address and updates the corresponding display location.

6.3.03 12-250V Converter (A16) - This converter provides the high voltage (+250V dc) required by the Self Scan * display.

U1 is a dual monostable. 1/2 of U1 is used for generating a reset pulse which turns off the Self Scan * until the reset input has been removed for 100 ms. The other half of U1 forms a missing pulse detector which turns off Q1-Q2 if the Self Scan clock is removed either accidently or as a result of circuit fault. U2 is an encapsulated dc-dc converter which is non-serviceable.

6.4 Central Processing Unit

6.4.01 Data Input Control (A24) - The Data Input Control assembly contains four, 8 bit ports, two, 8 bit binary counters and address decoding circuits. Its primary function is to provide control and input lines for a number of time measurements in the T222C. The individual components and the lines controlled by this circuit can be seen in more detail on the schematic figure 8-37.

Address decoder U2, U3A, Q1 selects one of the four port I.C.'s (U6 thru U9) and either strobes the port's internal latch (U8) or enables the output buffers (U6, U7 and U9) under software control U3B, C and D. U1B and C are used to steer either a 10 KHz square wave used for time measurements or the input SF frequency into U5 - U4 for time or frequency measurements. U1A and D form an S-R flip flop which debounces the pulse data button under software control. Outputs from A24 include TIMER RESET which controls the A23 interrupt timer, and START CONV which controls the A/D conversion cycle on A26.

6.4.02 The CPU Assembly (A25) consists of an 8080 microprocessor, clock generator and buss interface, program PROMS and 512 bytes of program RAM. Refer to figure 8-39 and figure 6-2 as well as the simplified schematic figure 6-8.

* Burroughs Trademark

Clock generator U2 uses an 18 MHz crystal to generate the two phase 2 MHz CPU clock and also generates a reset signal from the front panel "clear" button. U3 is a buffer for the CPU data buss and generates memory read, write; it also generates an interrupt instruction. U12 is the address decoder for CPU memory. It disables all memory on A25 for addresses above 8000H (used by the Data Input Control). Memory on A25 is selected by the addresses shown on the schematic.

Detailed information on the 8080 system timing can be found in literature available from a number of sources such as Intel Corporation.

6.5 SF Analog Digital Interface

6.5.01 A/D CONVERTER & FREQUENCY DIVIDER (A26) - The A/D Converter & Frequency Divider Assembly performs two unrelated functions. It accepts an analog input of SF level from the A27 and converts to digital. It also contains a programmable frequency divider for SF generation.

U1, U2 and associated components form a buffer amp, a precision rectifier and a low pass filter. The dc level generated at U2-1 is input to log amp U3; the output of U3 is input to A/D converter U6 which converts the dc input level to an 8 bit binary number. This number is interfaced with the CPU data bus via U11 (a tri-state buffer) and address decoder U4. The A/D conversion cycle is controlled using the start converter input which originates at the Data Input Control Assembly, A24.

U7, U15, through U17 and parts of U14 form a programmable frequency divider. Programming is achieved by four groups of up to 11 diodes each that are selectively grounded by the front panel frequency select (SF FREQ) thumbwheel switch. The output at Y is a square wave whose frequency is equal to the S.F. frequency.

6.5.02 SF Send Receive Detector (A27) - The SF Send Receive Detector is used to interface SF type circuits to the pulse measurement circuitry of the T222C. Included on the same assembly is the low pass filter and AGC circuitry for the generation of SF tone for the T222C send section.

U1 provides a balanced input to the S.F. receive detector. R3 provides a null adjustment used to cancel any common mode signals (i.e. hum) which may be present. U2A, B forms two low pass filters. U2B has a high cutoff frequency; it is used for level measurement by the A/D converter-frequency divider board. U2A has a low cutoff (approx 6 KHz); its output feeds comparators U3 and U4. The outputs of U3 and U4 are used by dual edge-triggered mono U5. U4 and Q2 set the receive threshold for the set. Q2 is controlled by the front panel REC INTERFACE, SF/FROM LINE push button switches.

U5 provides a pulse validation window for rejection of spurious pulses. Q1 acts as a buffer for the U5 output which feeds into the receive interface switches. The received SF frequency output (U3-7) indicates the presence of SF to the Data Input Control board.

U6 and U7A form a six pole low pass filter that smoothes and removes clock components from the square wave at pin 19 which originates at the A/D converter-frequency divider board. Q3, U8 and U9 form an AGC circuit which provides a stable, temperature compensated output level. U7B is a unity gain buffered tone output used for reverse supervision.

6.5.03 SF Attenuator (Part of A15) - The active circuits for the front panel SF LEVEL thumbwheel switches are located on this assembly. The output from the tone level attenuator is buffered and amplified by U1A and applied to the unit's attenuator. U1B is a unity gain buffer for the unit's attenuator. Base drive for both Q1 and Q2 comes from A30.

6.6 Send Interface and Receive Interface Controls

6.6.01 Receive, Pulsing Type (A5) - This control assembly determines the routing of receive pulsing from the individual interface circuits.

6.6.02 Send Pulse Type Control (A7) - This control assembly determines the routing of out pulsing to the individual interface circuits.

6.6.03 Control assemblies A5 and A7 also provide DX reverse supervision switching to DX Supervision assembly A14 as well as status input to the CPU and SF operation.

6.7 Loop and Line Pulser

6.7.01 The Loop and Line Pulser (A17) contains the -48 Volt Regulator, the dc Loop Pulser, the M Lead Pulser, E Lead Pulser and the DX Pulser circuitry. The make/break signal is supplied by assembly A21.

-48 Volt Regulator (Q10) senses the voltage drop across R21 and R22 and turns on the SHORT lamp if the -48 volt supply current exceeds approximately 170 ma. Q13 is a difference amplifier that controls base drive to Q11; therefore, it controls the output voltage. Q12 functions as a foldback limiter protecting series pass element Q11 if excess current is drawn. Q14, Q15 and Q16 form a similar regulator circuit where the -48 volt supply is used internally by other than the pulser circuitry.

6.7.02 Loop Pulser (Q1 and Q2) drives opto isolator U1 which provides isolated drive to Q4. Q3 and Q4 are in a diode bridge configuration that allows for a bi-polar loop closure using a single pass element.

6.7.03 Loop Battery Ground Pulser (Q5 and Q6) provides level shifted base drive for Q7 and Q8; Q8 provides base drive for Q9.

6.7.04 E and M Pulsers

A. M Lead Pulser (Q19 and Q20) provides level shifted drive for Q18 which is the pass element to ground. Q17 protects Q18. In a similiar manner Q21 and Q22 drive Q23 which supplies -48 volts to the M - LEAD.

B. E Lead Pulser (Q24 through Q26) provides level shifted and base drive for pass element Q27. Q28 provides limiting.

6.7.05 DX Pulser (Q29 and Q30) provides level shifted drive for Q34 which is the pass element to ground. Q35 protects Q34. In a similiar manner Q31 and Q32 drive Q33 which supplies -48 volts to DX PULSER OUT.

6.8 Signaling Send Receive Interface Circuits

There are four signaling interface circuits discussed in this section. A detailed description of all the control circuit combinations would not serve a useful purpose. Therefore, only those circuits containing active components are described. The Simplified Schematics in this section can be cross referenced with the detailed schematics of section 8.0 if detailed circuit tracing is required. The "A" number code will simplify cross referencing.

6.8.1 Loop Signaling: Send/Receive Interface

6.8.1.01 The Loop Signaling: Send/Receive Interface includes part or all of each of the listed circuit or control assemblies.

1. Receive Interface Control - A6
2. Send Pulse Type Control - A7
3. Loop Detector Circuit - A18
4. Leak Conditions (and SF Impedance) Circuits - A9
5. Loop and Line Pulser Circuits - A17
6. Send Interface Control - A11
7. Loop Resistance (and Send Control) Circuits - A8

The Loop Detector Circuit (A18) is described in Section 6.8.1.02. The Loop Pulser and the Loop Battery Ground Pulser circuits were covered in Section 6.7.02 and Section 6,7.03. The Loop Resistance Circuit (A8) and the Leak Conditions Circuit (A9) provide the Line characteristics required for loop signaling. The pulse, SEND/RECEIVE directions are determined by the LOOP: INPUT/OUTPUT jacks and the associated "CONTROLS" push buttons figure 3-1.

6.8.1.02 Loop Detector (A18) - This assembly provides dc loop to logic level conversion, -48 volt battery feed and the "A" relay simulator circuitry.

U1 forms a dual comparator which senses voltage changes across battery feed resistors R14 and R7. The difference between the two outputs of U1 is summed at U2. The second half of U2 compares the dc level generated by the first half to a reference voltage determined by a series resistance that includes R29. R29 is used to adjust the terminated % Break and Speed display at 12 PPS and 60% Break. Q1 and Q2 level shift U2's output for TTL compatibility. Comparators U3 and U4 form the bridged loop detector. Tip-Ring differential pass through diode bridge CR5 - CR8 (figure 8-28), is current limited and then buffered by ½ U3. The second half of U3 forms a low pass filter which rejects spurious pulses outside nominal % Break and Speed ranges. This band limited output is compared by ½ U4 against reference voltage generated across a resistance that includes R47. R47 is provided for calibration.

6.8.2 DX Signaling: Send/Receive Interface

6.8.2.01 The DX Signaling Send/Receive Interface includes all or part of each of the circuit or control assemblies listed.

1. DX Supervision Circuit - A14
2. Receive Pulsing Type Control - A5
3. Receive Interface Control - A6
4. Send Interface Control - A11
5. Loop and Line Pulser Circuits - A17
6. Send Pulse Type Control - A7
7. Loop Resistance & Send Control - A8

The DX Supervision Circuit (A14) is described in Section 6.8.2.02. The Pulser Circuit was covered in Section 6.7.05. The DX Interface Control circuits and the Send/Receive Interface Control switching determine the direction for out pulsing and for receiving.

6.8.2.02 DX Supervision (A14) - This assembly provides interface between T222C internal logic and DX type circuits. Q7-Q11, U1 and U2 form the A/B reversal detector. Q6 and Q5 provide a 250 ohm impedance DX detector and drive Q12 providing the DX on hook signal as well as driving the DX on-hook LED. Q1 and Q2 comprise the high impedance on hook detector while Q3 and Q4 form the off hook condition DX detector. These are switched depending on whether or not the receiving end is on or off hook.

6.8.3 E & M Signaling: Send/Receive Interface

6.8.3.01 The E & M Interface Circuits determine the pulsing and receiving directions (outpulsing and detection). The Send/Receive Interface includes all or parts of the circuits and controls listed:

1. Loop and Line Pulser Circuits - A17
2. E & M Supervision Circuit - A12
3. Send Interface Control - A11
4. Receive Interface Control - A6

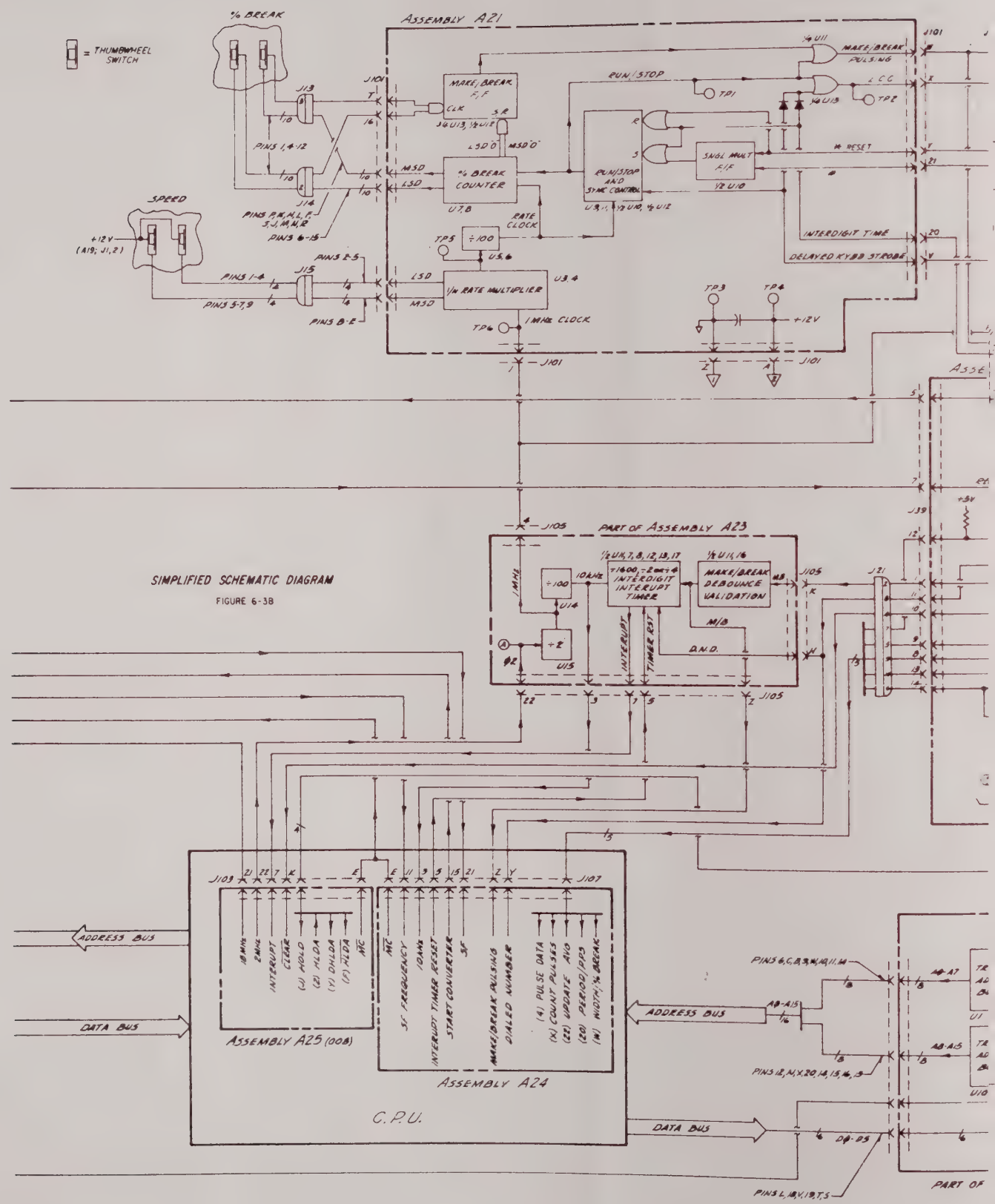
The Loop and Line Pulser Circuits were described in Section 6.7.04; the E & M Supervision are described in Section 6.8.3.02. The switching control circuits determine the direction for pulsing and receiving as well as select the monitor or terminating circuits.

6.8.3.02 E & M Supervision (A12) - provides supervision for E and M type pulsing where normal E conditions are open-idle and ground seized, and normal M conditions are ground idle and battery seized.

Q5, 6, 7 form a high impedance battery detector used in the MON mode. Q8 thru Q10 form the terminated lead detector which provides a 470 ohm termination for the signaling equipment under test.

Q3 and Q4 form a high impedance ground detector for use in the MON mode. Q1 and Q2 form the terminated E lead ground detector which provides a 470 ohm termination for the equipment under test.

6.9 Power Supply (A19) - The T222C power supply is a conventional linear supply using discrete diodes bridges and filter capacitors for rectification and three terminal I.C. voltage regulators for the required supply voltages.


= THUMBWHEEL SWITCH
% BREAK
SPEED
+12V (A19; J1,2)
PINS 1,4,12
PINS P,R,N,L,E, S,J,M,H,C
PINS 6-15
PINS 1-4
PINS 5-7,9
PINS 2-5
PINS B-E
J13
J14
J15
J101
ASSEMBLY A21
MAKE/BREAK F/F
CLK
S.R
MSD
LSD
% BREAK COUNTER
U7,8
RATE CLOCK
÷100
U5,6
1/n RATE MULTIPLIER
U3,4
1 MHz CLOCK
TP5
TP6
RUN/STOP
TP1
TP2
RUN/STOP AND SYNC CONTROL
SNGL MULT F/F
½ U10
MAKE/BREAK PULSING
M RESET
INTERDIGIT TIME
DELAYED KYBD STROBE
TP3
TP4
+12V
PART OF ASSEMBLY A23
÷100
÷2
U14
U15
1 MHz
10 kHz
÷1600, =2 or =4 INTERDIGIT INTERRUPT TIMER
MAKE/BREAK DEBOUNCE VALIDATION
INTERRUPT
TIMER RST
M/B
D.N.D.
J105
J21
+5V
J39
SIMPLIFIED SCHEMATIC DIAGRAM
FIGURE 6-38
ADDRESS BUS
DATA BUS
J109
J107
ASSEMBLY A25 (008)
ASSEMBLY A24
C.P.U.
10 kHz
2 kHz
INTERRUPT
CLEAR
(J) HOLD
(2) HLDA
(Y) DMLDA
(7) HLDA
INC
5F FREQUENCY
10 kHz
INTERVAL TIMER RESET
START CONVERTER
5F
MAKE/BREAK PULSING
DIALED NUMBER
(4) PULSE DATA
(N) COUNT PULSES
(22) UPDATE A/D
(20) PERIOD/PPS
(M) WIDTH/% BREAK
PINS 6,C,B,3,M,Q,11,M
PINS 12,N,X,20,14,15,4,3
A0-A7
A8-A15
DATA BUS
D0-D5
PINS L,A,V,19,T,S
PART OF

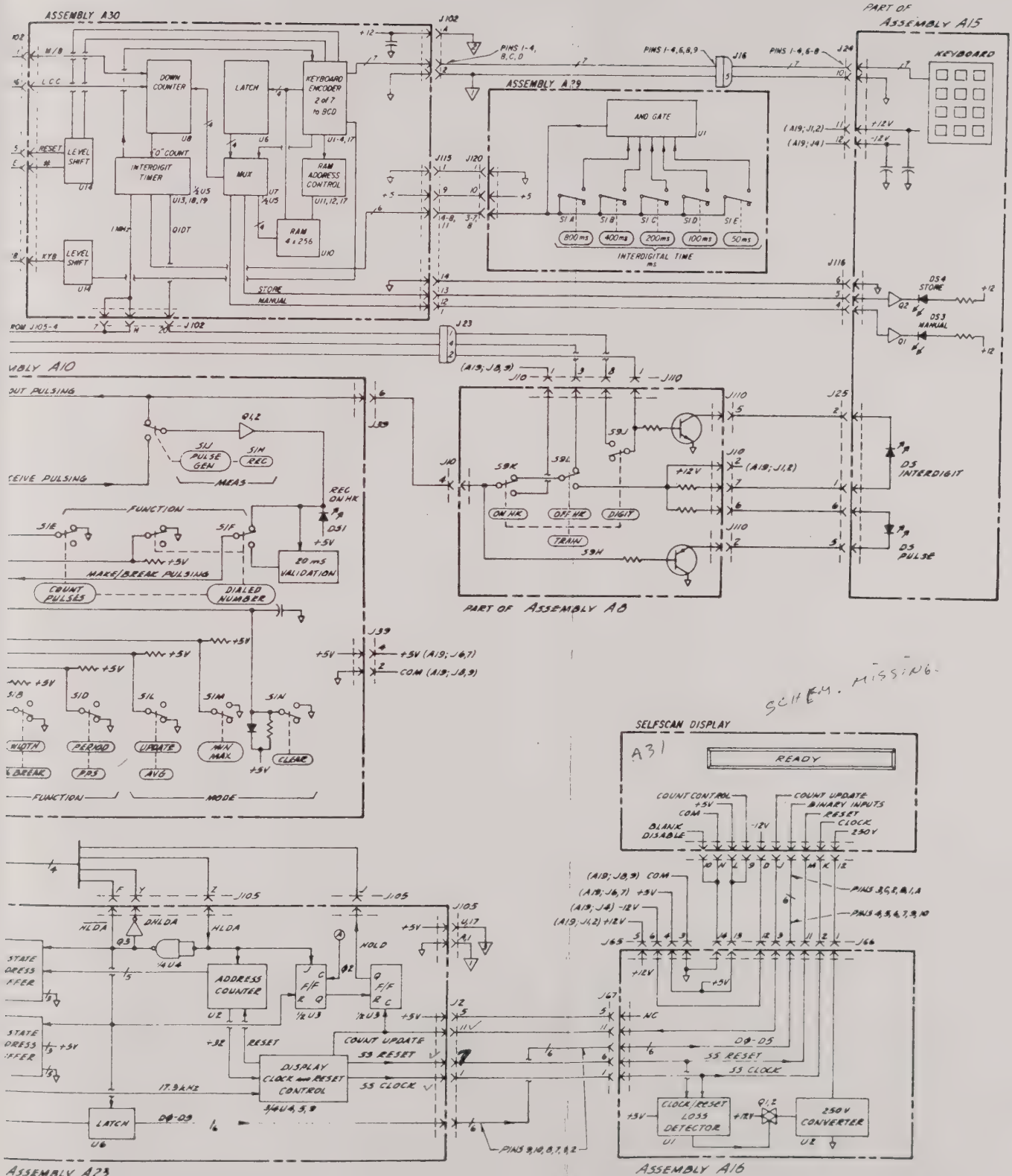
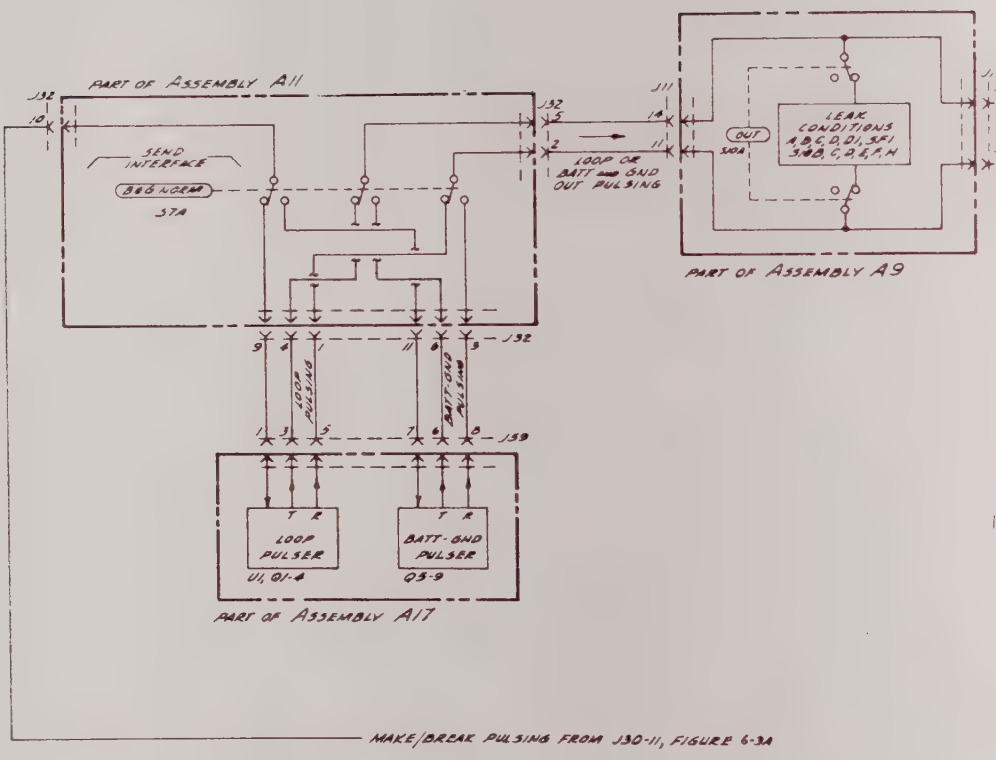
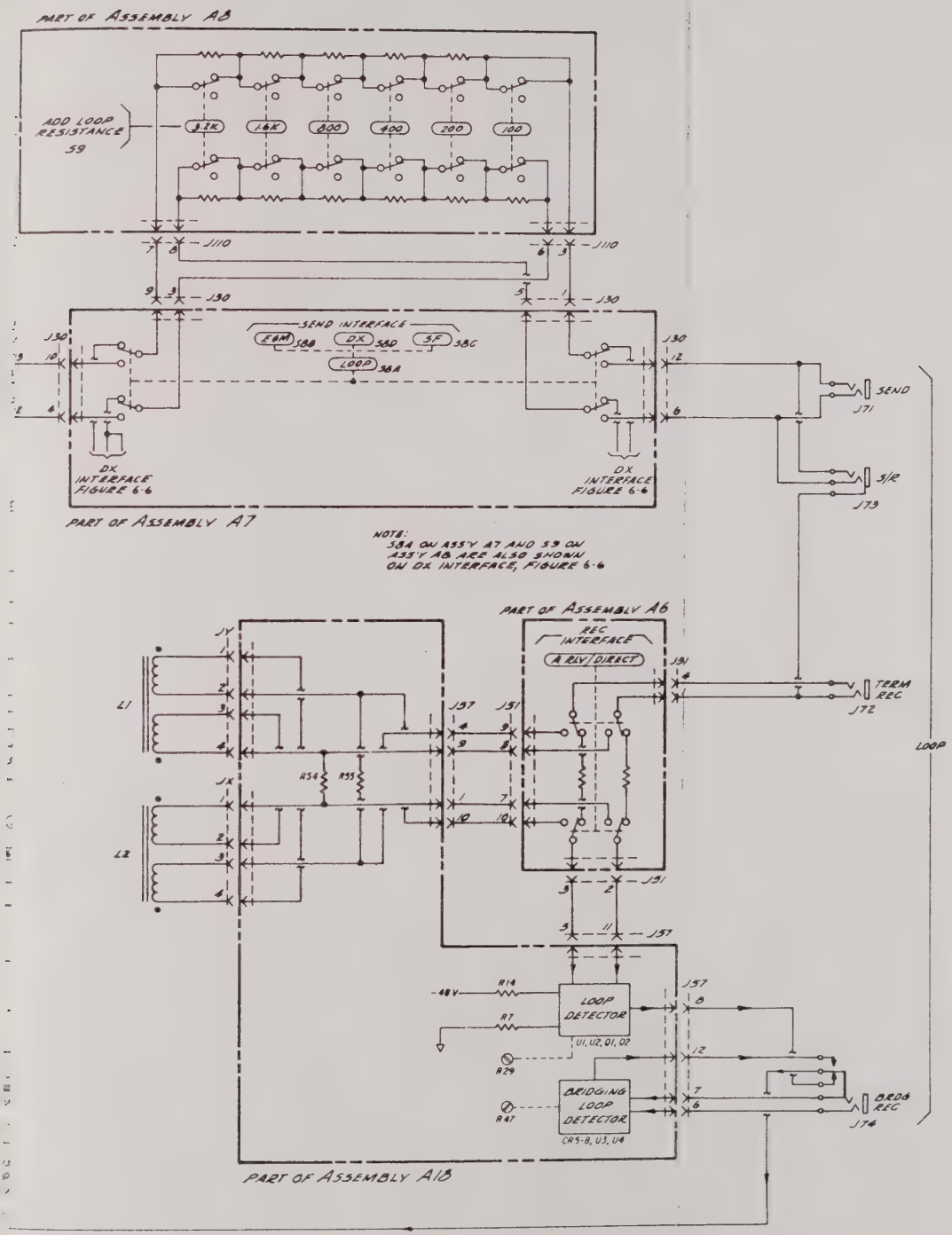


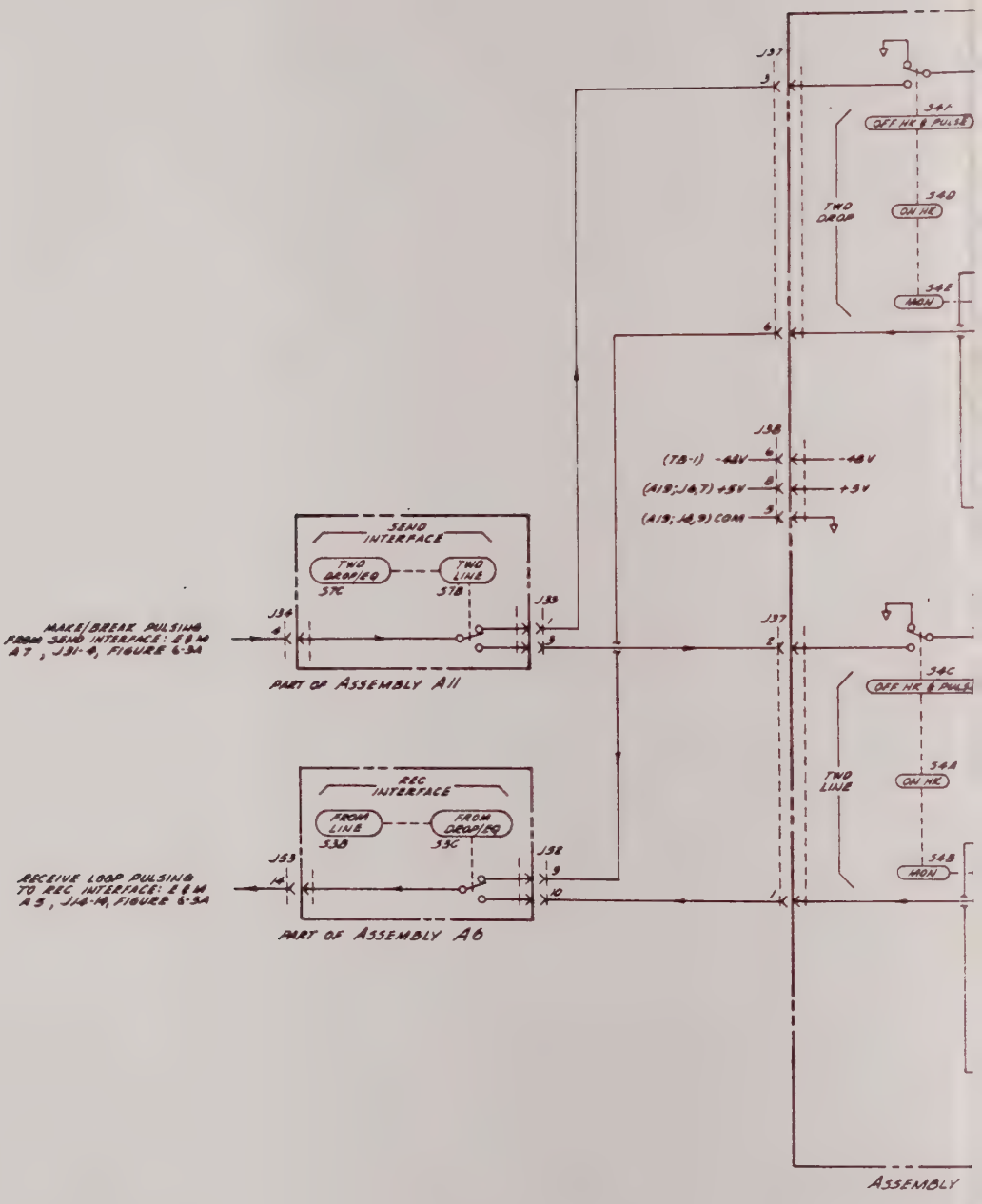
FIGURE 6-3B
Simplified Schematic

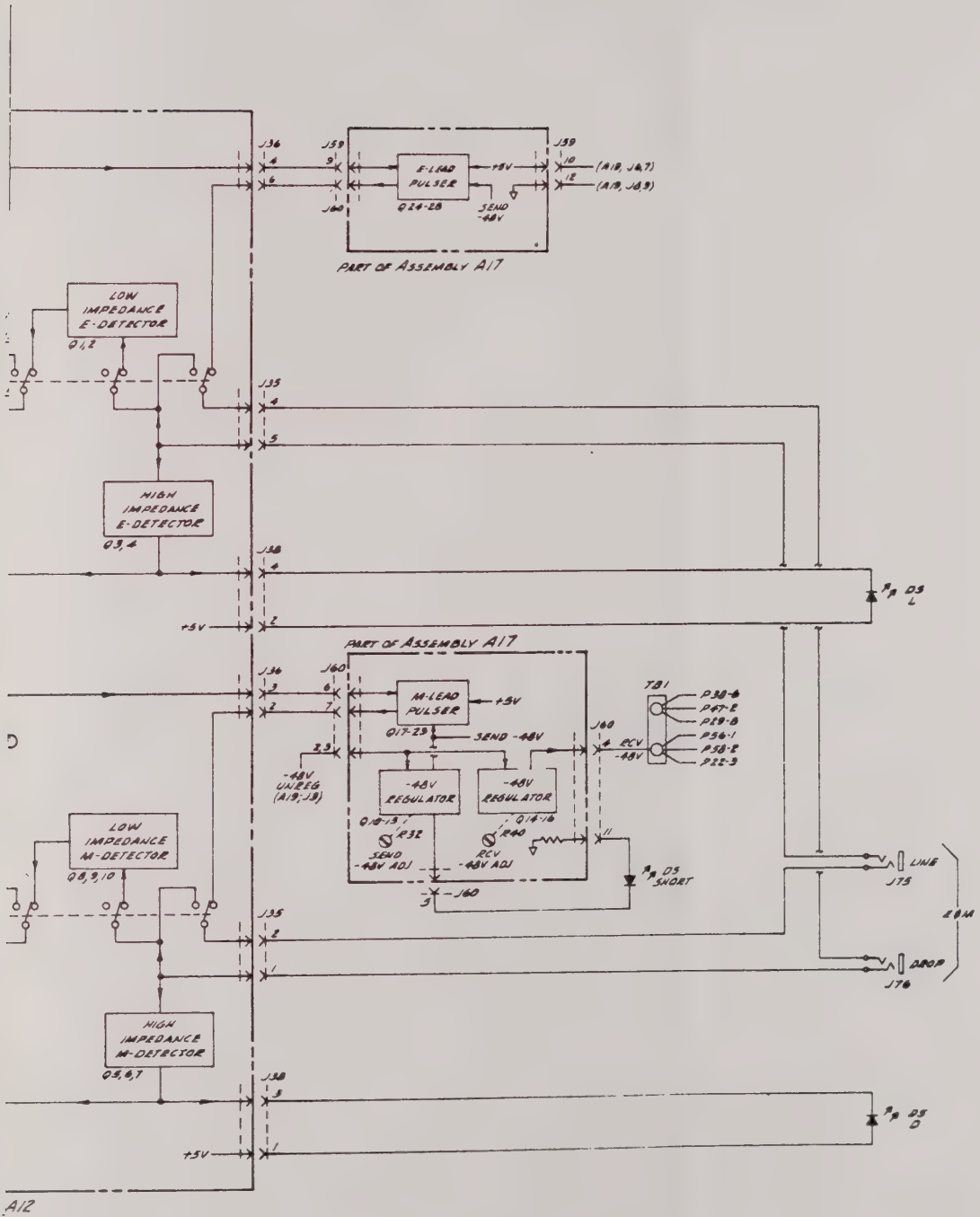

PART OF ASSEMBLY A11
J32
10
SEND INTERFACE
B&B NORM
S7A
J32
5
2
LOOP OR BATT and GND OUT PULSING
J11
14
11
OUT
S10A
LEAK CONDITIONS A, B, C, D, D1, SF1, 3, 4B, C, E, F, H
PART OF ASSEMBLY A9
9
4
1
11
6
3
J32
LOOP PULSING
BATT-GND PULSING
1
3
5
7
6
8
J39
T
R
LOOP PULSER
U1, Q1-4
T
R
BATT-GND PULSER
Q5-9
PART OF ASSEMBLY A17
MAKE/BREAK PULSING FROM J30-11, FIGURE 6-3A
RECEIVED LOOP PULSING TO J56-B, FIGURE 6-3A



LOOP INTERFACE

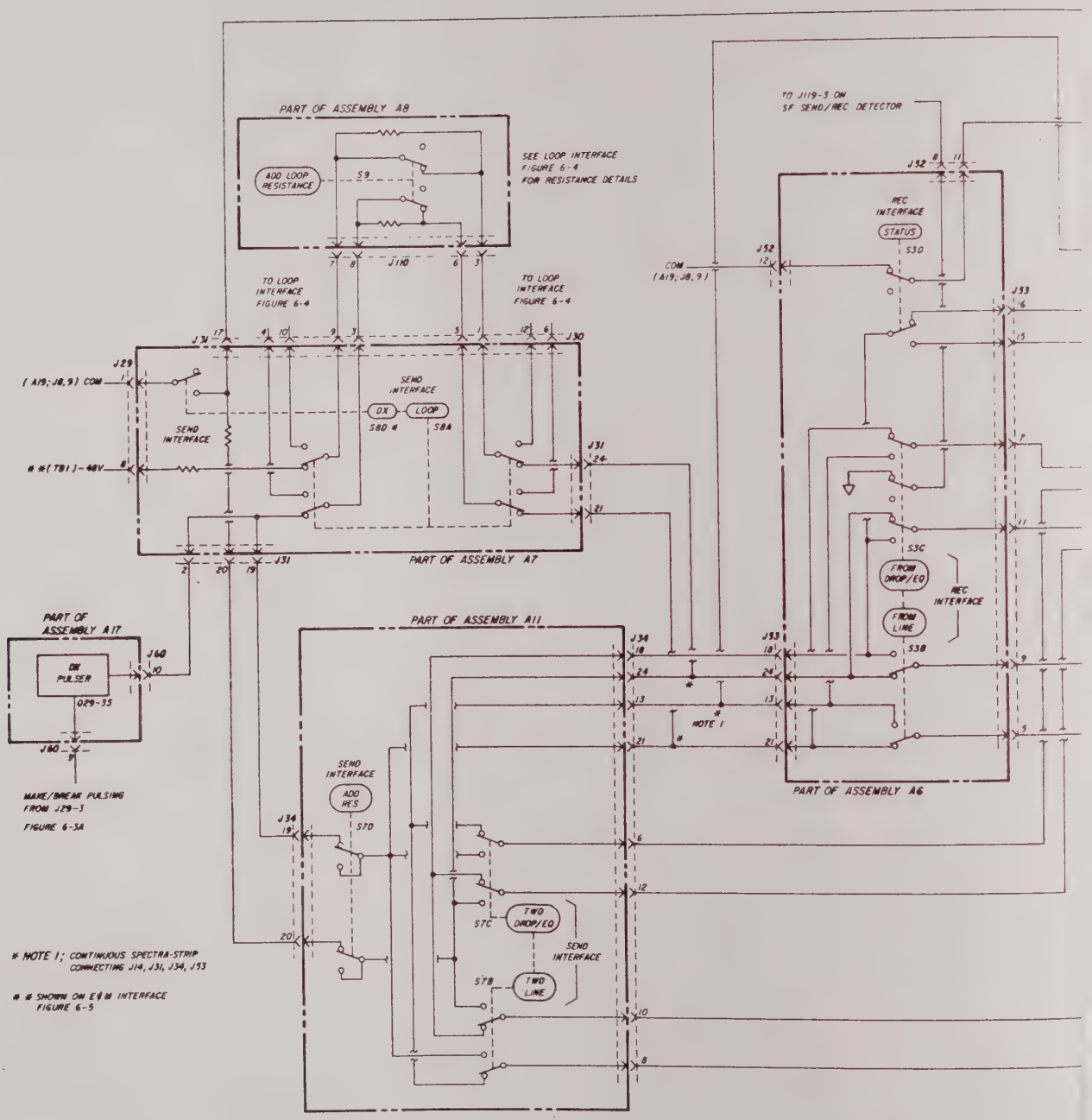
FIGURE 6 4

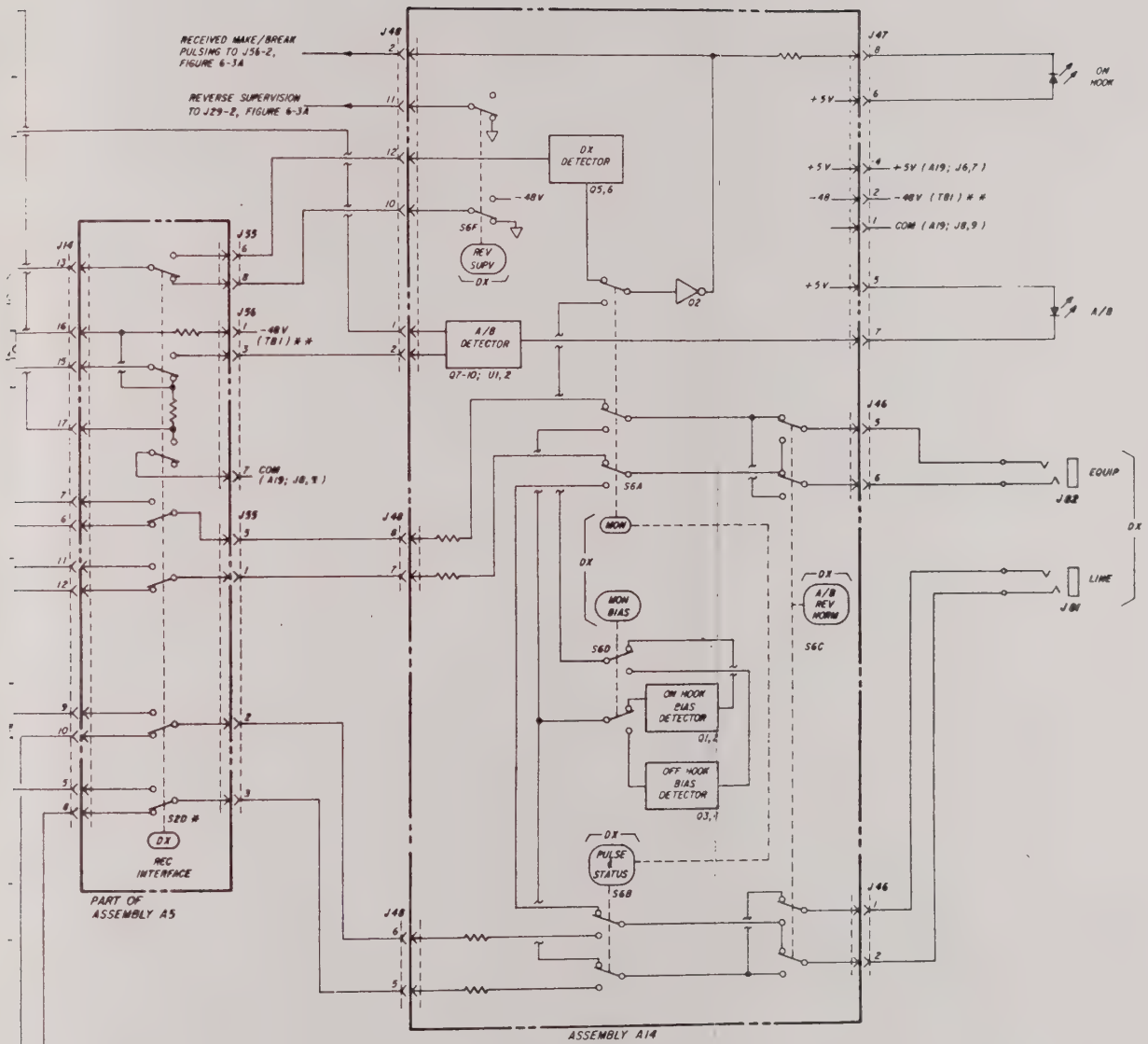

J37
3
341
OFF HK & PULSE
340
ON HK
TWO DROP
345
MON
6
J38
(TB-1) -48V
-48V
(A19; J4,7) +5V
+5V
(A19; J4,9) COM
SEND INTERFACE
TWO DROP/EQ
TWO LINE
STC
STB
J33
J34
4
MAKE/BREAK PULSING FROM SEND INTERFACE: E & M A7, J31-4, FIGURE 6-3A
PART OF ASSEMBLY A11
J37
2
34C
OFF HK & PULSE
34A
ON HK
TWO LINE
34B
MON
REC INTERFACE
FROM LINE
FROM DROP/EQ
SSB
SSC
J32
J39
14
9
10
1
RECEIVE LOOP PULSING TO REC INTERFACE: E & M A5, J14-14, FIGURE 6-3A
PART OF ASSEMBLY A6
ASSEMBLY



E&M INTERFACE

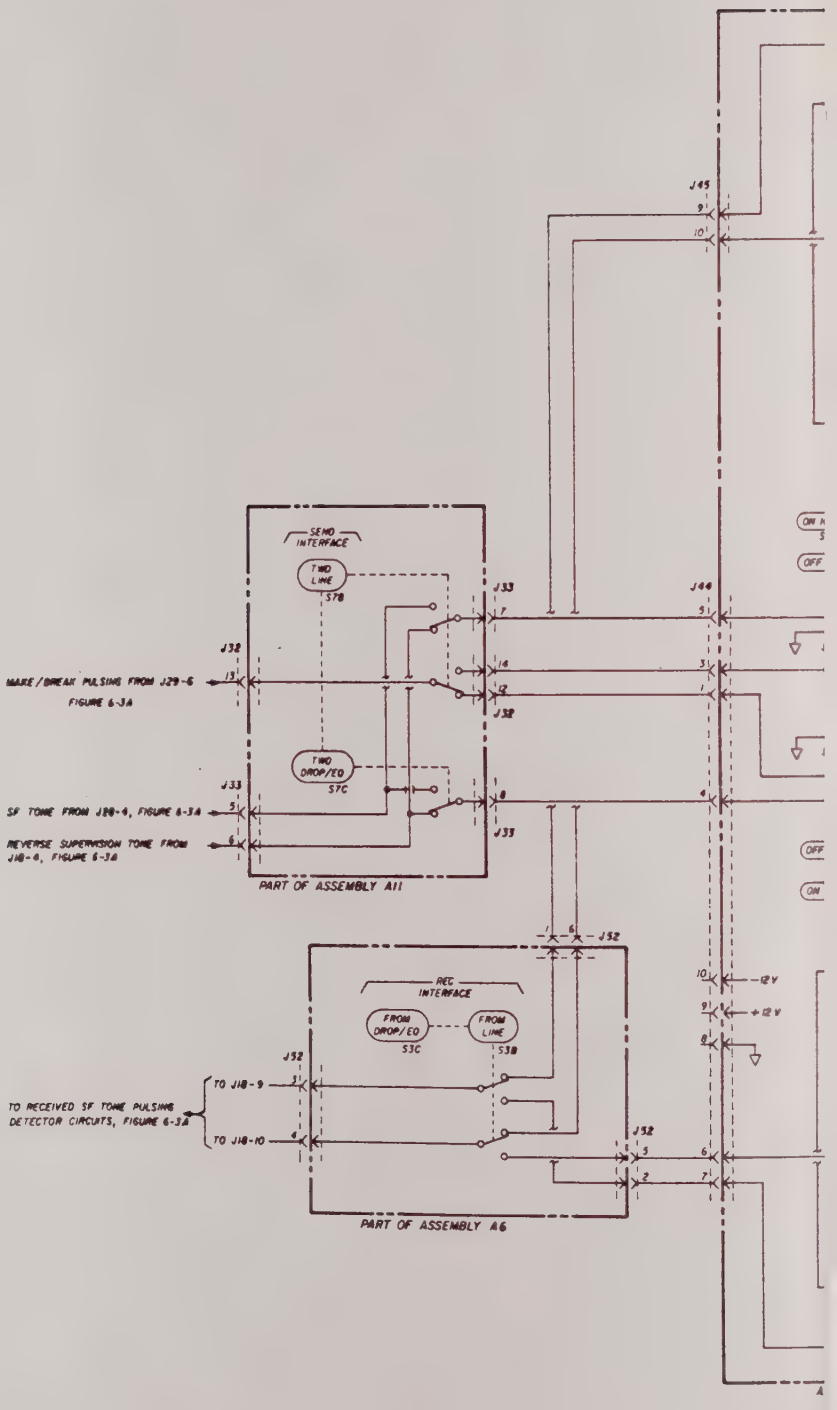
FIGURE 6-5

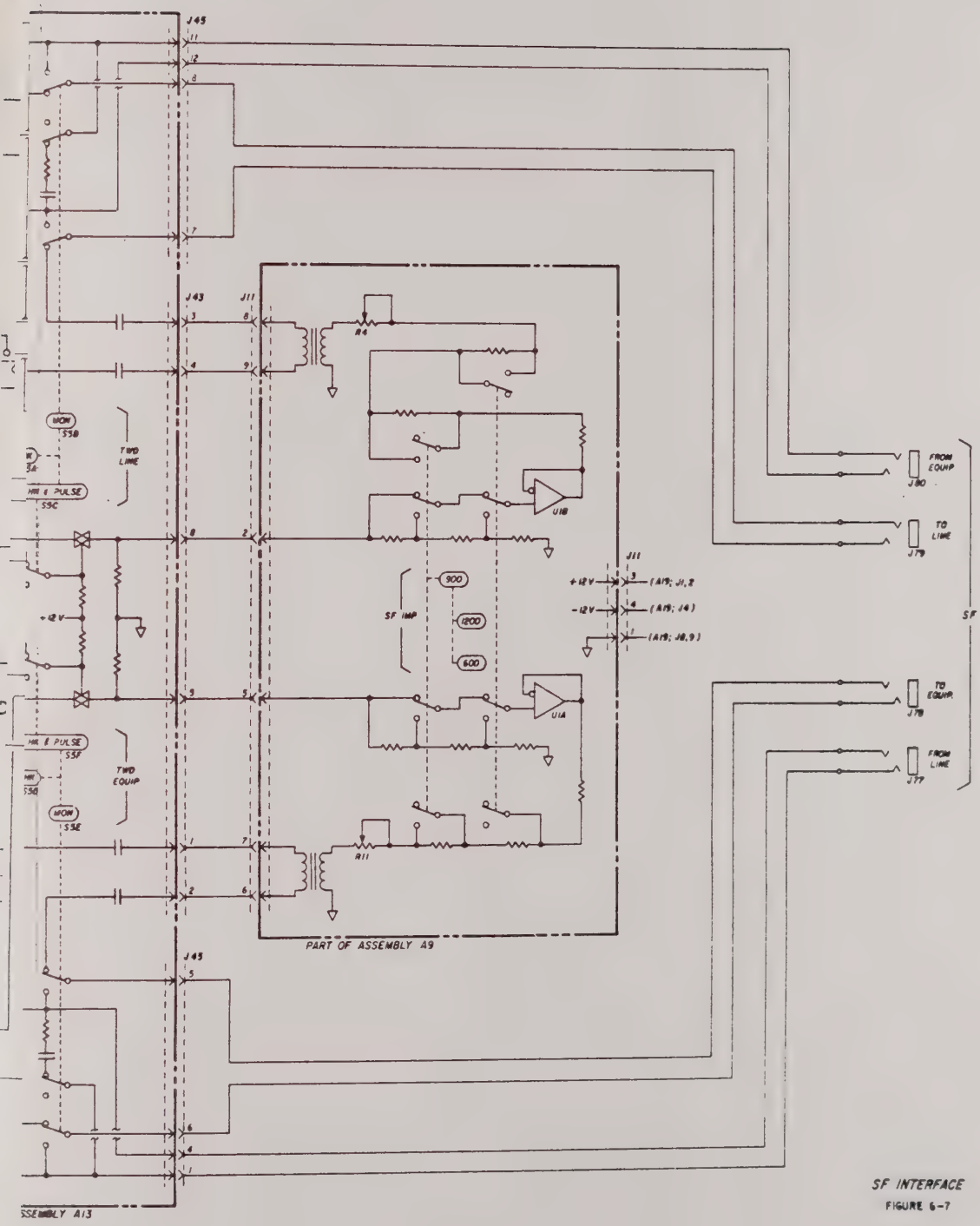

PART OF ASSEMBLY A8
ADD LOOP RESISTANCE
S9
SEE LOOP INTERFACE FIGURE 6-4 FOR RESISTANCE DETAILS
J110
TO LOOP INTERFACE FIGURE 6-4
TO LOOP INTERFACE FIGURE 6-4
J31
J30
J29
(A19; J8, 9) COM
SEND INTERFACE
SEND INTERFACE
DX
LOOP
S8D
S8A
#(TB1)-48V
PART OF ASSEMBLY A7
PART OF ASSEMBLY A17
DX PULSER
J60
029-35
MAKE/BREAK PULSING FROM J29-3 FIGURE 6-3A
PART OF ASSEMBLY A11
SEND INTERFACE
ADD RES
S7D
S7C
TWO DROP/EQ
SEND INTERFACE
S7B
TWO LINE
NOTE 1; CONTINUOUS SPECTRA-STRIP CONNECTING J14, J31, J34, J53
SHOWN ON E&M INTERFACE FIGURE 6-5
TO J119-3 ON SF SEND/REC DETECTOR
J52
REC INTERFACE
STATUS
S3D
COM (A19; J8, 9)
J53
S3C
FROM DROP/EQ
FROM LINE
REC INTERFACE
S3B
NOTE 1
PART OF ASSEMBLY A6



DX INTERFACE

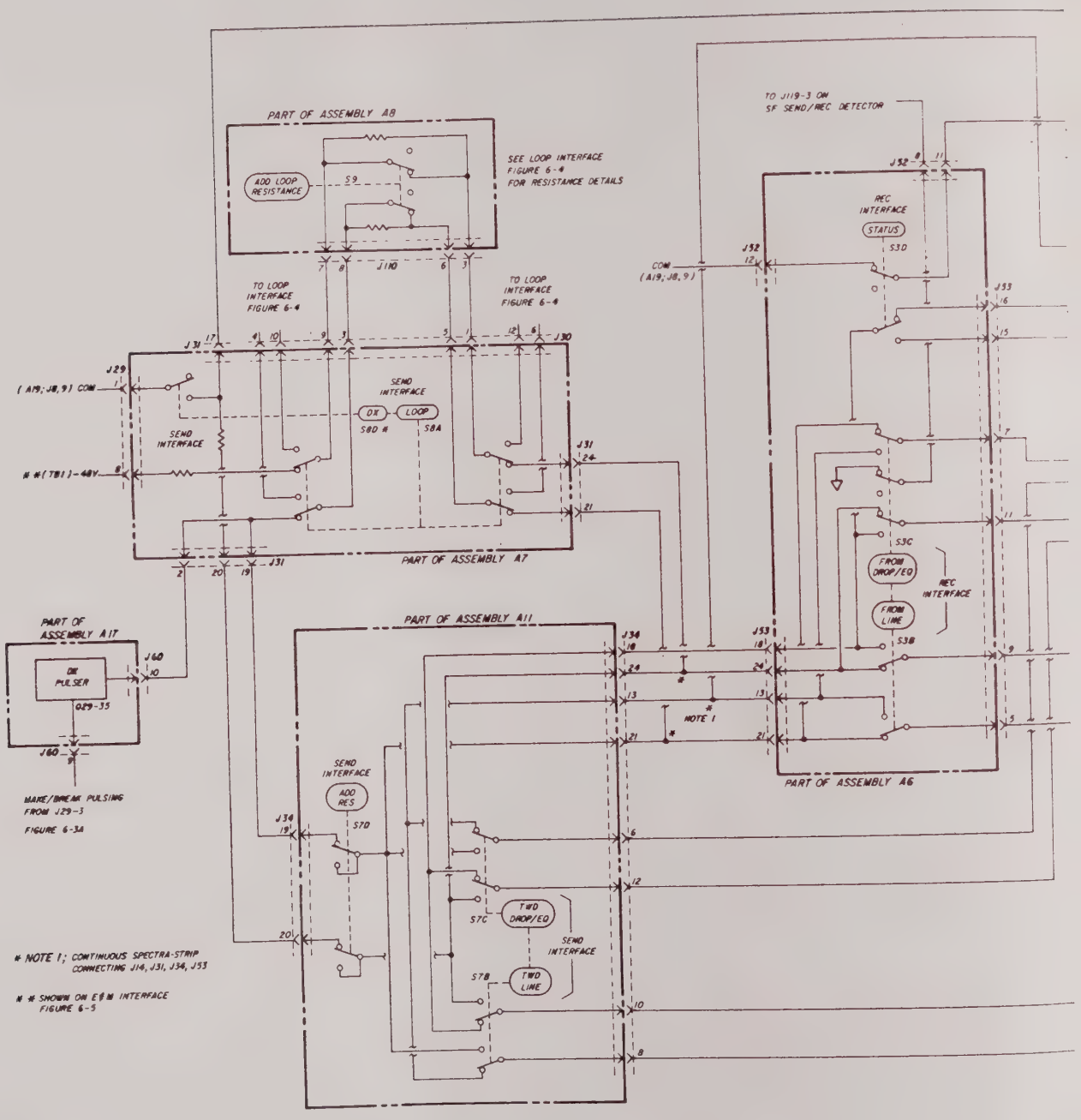
FIGURE 6-6

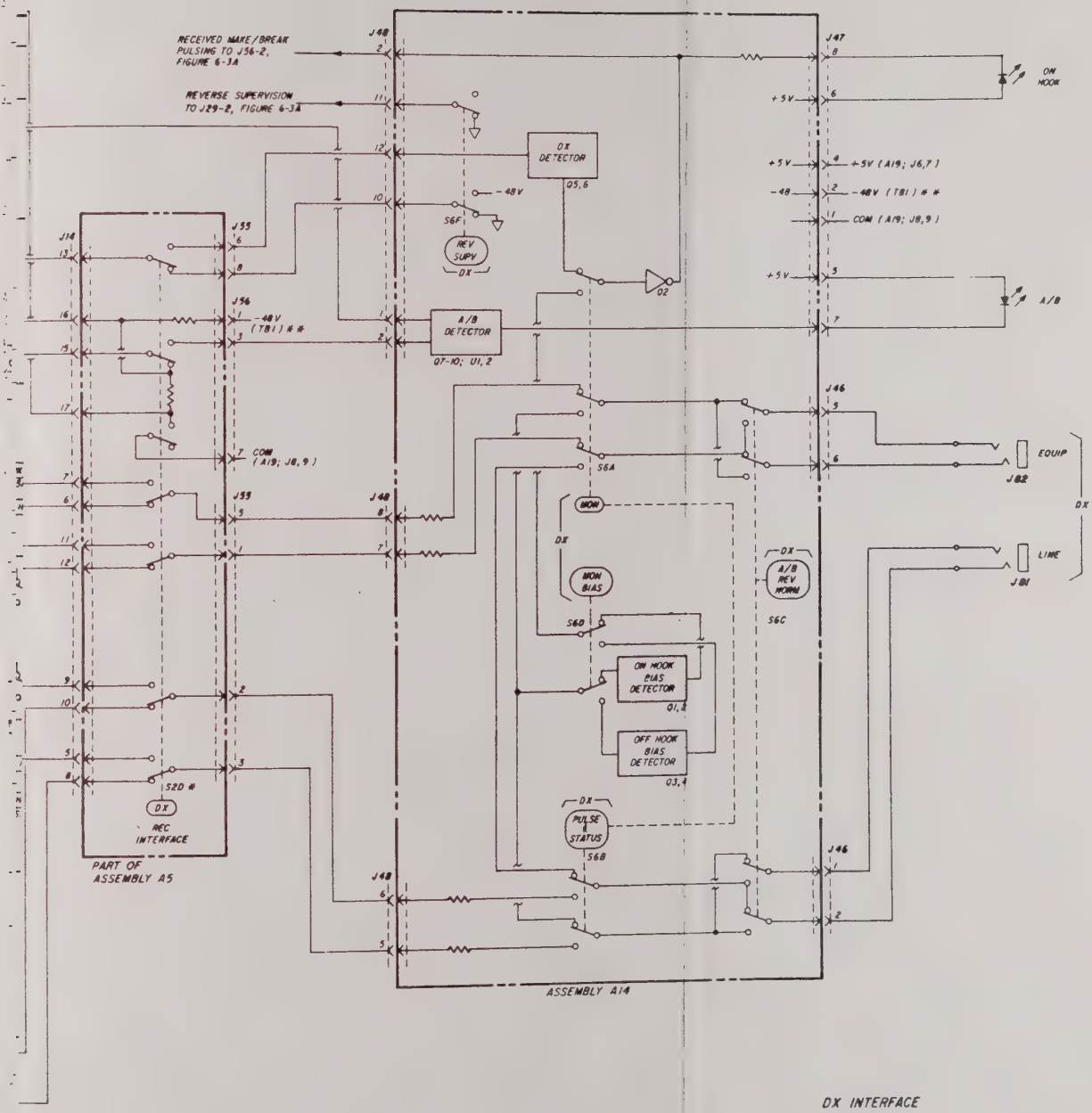

SEMD INTERFACE
TWD LINE
S7B
TWD DROP/EQ
S7C
J33
J32
J44
J45
MAKE/BREAK PULSING FROM J29-6
FIGURE 6-3A
SF TONE FROM J28-4, FIGURE 6-3A
REVERSE SUPERVISION TONE FROM J18-4, FIGURE 6-3A
PART OF ASSEMBLY A11
REC INTERFACE
FROM DROP/EQ
S3C
FROM LINE
S3B
TO J18-9
TO J18-10
TO RECEIVED SF TONE PULSING DETECTOR CIRCUITS, FIGURE 6-3A
PART OF ASSEMBLY A6
-12 V
+12 V
ON
OFF



SF INTERFACE

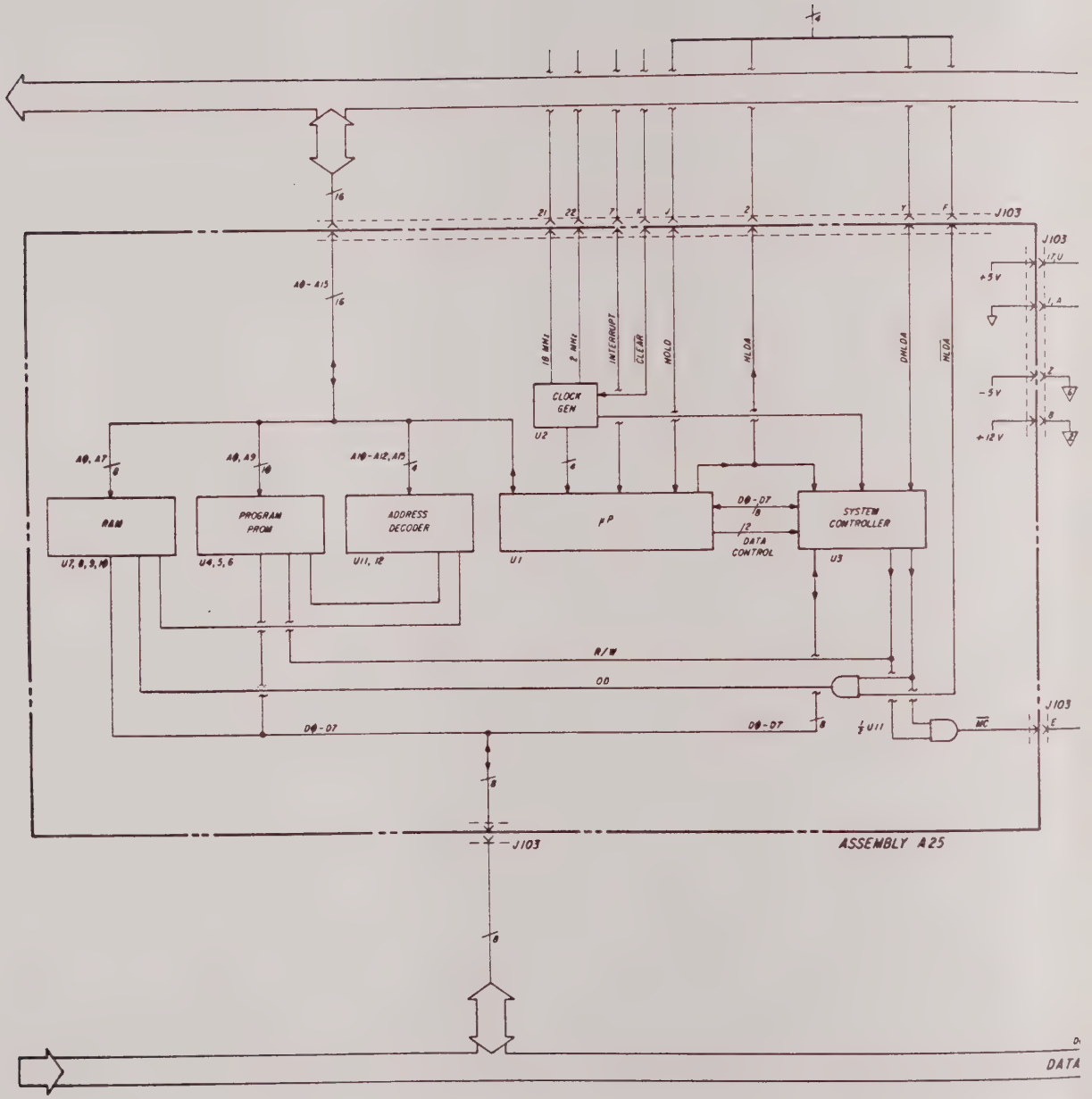
FIGURE 6-7

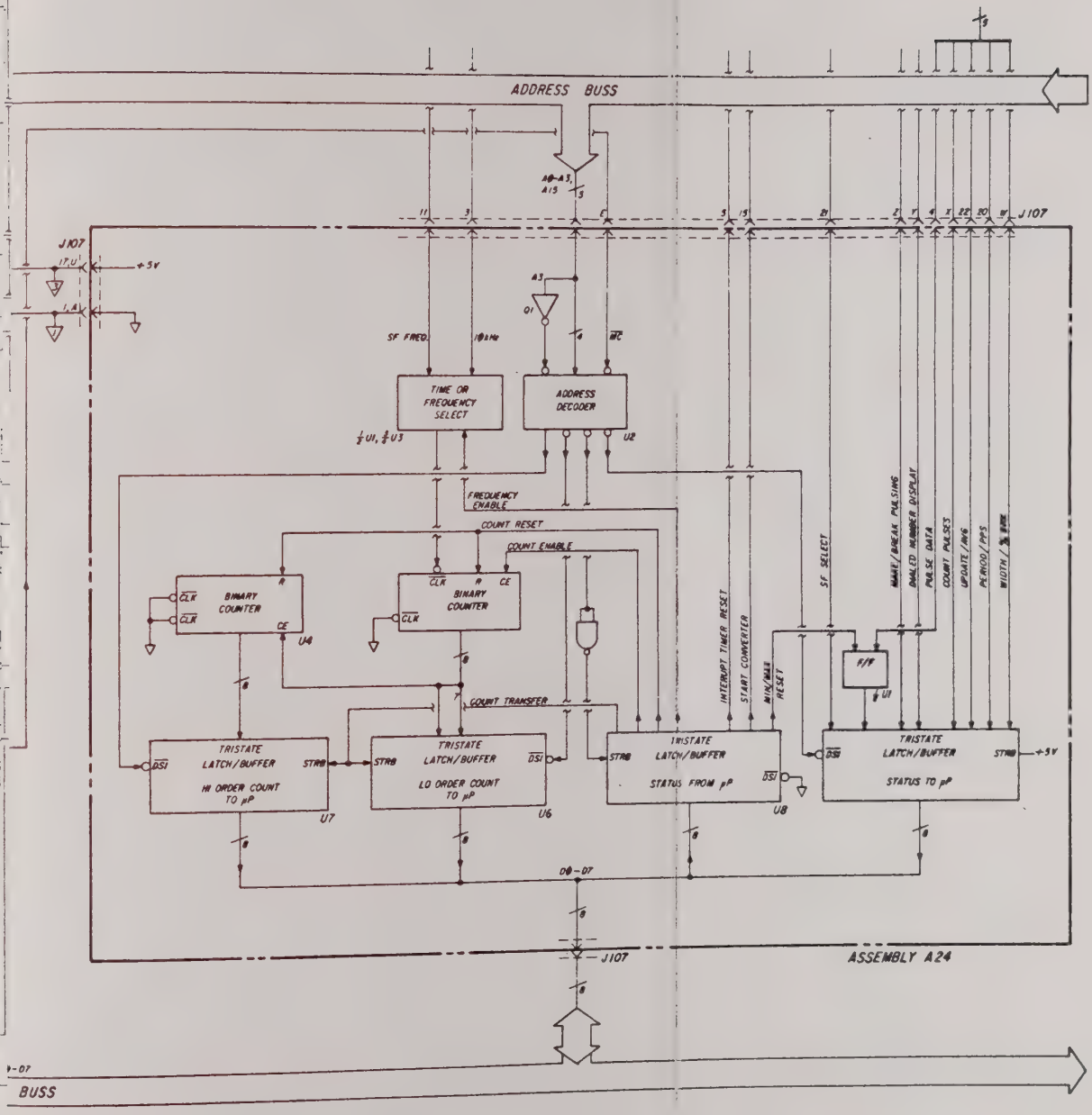

PART OF ASSEMBLY A8
ADD LOOP RESISTANCE
S9
SEE LOOP INTERFACE FIGURE 6-4 FOR RESISTANCE DETAILS
J110
TO LOOP INTERFACE FIGURE 6-4
TO LOOP INTERFACE FIGURE 6-4
TO J119-3 ON SF SEND/REC DETECTOR
J32
REC INTERFACE
STATUS
S3D
COM (A19; J8, 9)
J33
J31
J30
J29
(A19; J8, 9) COM
SEND INTERFACE
SEND INTERFACE
DX
LOOP
S8D #
S8A
#(TB1)-48V
J31
PART OF ASSEMBLY A7
S3C
FROM DROP/EQ
FROM LINE
REC INTERFACE
S3B
PART OF ASSEMBLY A11
PART OF ASSEMBLY A17
DX PULSER
J60
D29-35
J60
MAKE/BREAK PULSING FROM J29-3
FIGURE 6-3A
J34
J53
NOTE 1
PART OF ASSEMBLY A6
SEND INTERFACE
ADD RES
S7D
J34
S7C
TWD DROP/EQ
SEND INTERFACE
S7B
TWD LINE
NOTE 1; CONTINUOUS SPECTRA-STRIP CONNECTING J14, J31, J34, J53
SHOWN ON E&M INTERFACE FIGURE 6-5



DX INTERFACE

FIGURE 6-6


J103
A0-A15
16
18 MHz
2 MHz
INTERRUPT
CLEAR
WOLD
HLDA
DMLDA
+5V
-5V
+12V
CLOCK GEN
U2
A0, A7
A0, A9
A10-A12, A15
RAM
U7, 8, 9, 10
PROGRAM PROM
U4, 5, 6
ADDRESS DECODER
U11, 12
FP
U1
D0-D7
DATA CONTROL
SYSTEM CONTROLLER
U3
R/W
DD
D0-D7
U11
MC
J103
ASSEMBLY A25
DATA



C.P.U.

FIGURE 6-8

7.0 MAINTENANCE

7.1 General

7.1.01 All Wilcom Products, Inc. Test Equipment is warranted against defects in materials and workmanship for a period of one year from the date of delivery. Complete details of the warranty can be found on the title page of this manual.

7.1.02 Field repair of this test set is NOT recommended unless the repair will be made in a well equipped repair center. The technicians performing the repair should be familiar with microprocessor based test equipment, digital circuitry, logic functions and state of the art semiconductor design.

7.1.03 In the event of troubles, it is important that the Operational Checks described in 5.0 be performed BEFORE any attempts are made to repair the test set. By following this procedure, it can be determined if the problem is real or results from improper operation of the test set.

7.1.04 If trouble occurs that cannot be located by following the procedures of Section 5.0 and corrected by following the procedures of Section 7.2, reference can be made to the circuit description of Section 6.0 for a more detailed analysis.

7.1.05 If local repair is not possible, it is suggested that the complete test set be returned for repair with information regarding the suspected trouble.

7.1.06 After any repairs, not made by Wilcom Products, Inc., the test set should be re-aligned. Section 7.3 Alignment and Calibration, describes the methods and equipment required. In most cases it will not be necessary to repeat the whole of this procedure, but only applicable portions.

7.2 Repair Procedure

7.2.01 The Operational Checks of 5.0 should give a good indication of the trouble location. The next step is to remove the set from its case.

CAUTION: DO NOT REMOVE ANY SCREWS FROM THE FRONT PANEL.

a. Remove the six 10-32 screws from the right and left sides and one 4-40 screw from the top middle of the front panel of the T222C. Grasping the two retractable black handles, lift the case wrap from the T222C chassis.

b. Loosen the two multi-turn knurled screw fasteners on the Rear Access Panel. Lay the Rear Access Panel back to make adjustments, test points and assemblies more accessible.

7.2.02 A good visual inspection may give a quick solution to the problem. Look for loose connectors, solder connections, or component parts which may have jarred loose or broken, or other visual clues. Pay particular attention to areas where the Operational Checks have indicated trouble.

7.2.03 If the fault is not apparent at this point, reference can be made to the schematic diagrams Section 8.0 and the circuit description of Section 6.0. The individual parts are identified in the P.C. Assemblies of Section 8.0. Refer to Section 7.11 for P.C. Assembly removal instructions and Photographs of P.C. Assembly locations.

7.3 Alignment and Calibration

7.3.01 This section provides information needed to align the Model T222C Signaling Test Set and to verify the proper operation of the set. Alignment information covers adjustments which can be made by field personnel, using standard test equipment.

7.3.02 The Operational Checks in Section 6 should be performed BEFORE any attempt is made to calibrate the Signaling Test Set. Malfunctions uncovered should be repaired prior to completion of this procedure.

7.3.03 Applying Power - To eliminate repetitive instructions, it is assumed that power will be removed from the T222C during all disassembly or assembly operations and reapplied prior to testing. Allow 5 minutes for circuits to stabilize each time power is applied.

7.3.04 The Case Wrap should be removed and the back panel released from the test set before starting the Alignment and Calibration Procedure (see Section 7.2.01).

7.3.05 While performing the Alignment and Calibration procedure, it may be necessary to extend some card cage P.C. assemblies to facilitate the adjustments and operations described. This is accomplished in the following manner:

1. Unscrew retainer and remove the PC assembly under test.
2. Insert the card extender (Wilcom part number 20005260) in its place.

   NOTE: The card extender fingers have been notched to allow insertion in any of the card cage PC positions.

3. Insert the PC assembly in the card extender's connector.

   CAUTION: Be careful to observe polarity of the PC assembly when inserting it in the extender.

7.4 Equipment Required

Electronic ac voltmeter or Level Meter accurate to within .1dB from 400Hz to 4kHz.

Digital Multimeter
General purpose oscillator - 400Hz to 4kHz; OdBm to -40dBm; low output impedance
dc supply - 44 volts
Frequency Counter
General Purpose Oscilloscope
Card Extender

7.5 Power Supply Checks

7.5.01 Using an ohmmeter, measure the resistance from chasis ground to the 115/230 Power Supply (A19) E6. (see Figure 8-29 , it should be <1 ohm).

NOTE: All future measurements (ac and dc) should be referenced to chassis ground unless otherwise noted.

7.5.02 Using a dc voltmeter, measure the voltage at each of the power distribution points, J1-J9, E12 and E19 of A19.

Reference Designation	Nominal Voltage
J1	+12
J2	+12
J3*	-70
J4	-12
J5	-5.2
J6	+5
J7	+5
J8,9	CKT COM
E12,13*	+20
E19*	-20

*NOTE: Voltages at these points are unregulated. The nominal voltages shown are rough approximations only.

7.5.03 Other Supplies

1. Using the dc voltmeter, measure the voltage at P/J 66 pin 1 of the 12-250V CONVERTER (A16). It should measure approximately 250 V.
2. Measure the "SEND" -48V supply voltage of the LOOP AND LINE PULSER (A17) at Q8 emitter. Adjust R32 (SEND VOLTAGE ADJUST) for - 50Vdc.
3. Measure the "RECEIVE" -48V supply voltage at P/J 60 pin 4 of A17. Adjust R40 (RECEIVE VOLTAGE ADJUST) for -50Vdc.

7.6 Initial Conditions

7.6.01 Engage the following push buttons:

DISPLAY CONTROL: FUNCTION: %BRK, PPS
DISPLAY CONTROL: MODE: MEAS: REC

DISPLAY CONTROL: MODE: UPDATE
ADD LOOP RESISTANCE: 400, 800
SEND CONTROL: ON HOOK
LEAK CONDITION: OUT, A
SF IMP: 900

7.6.02 Adjust the thumbwheel switches to the following position:

ADJUST SEND SIGNAL: SF LEVEL (-dBm): 00
ADJUST SEND SIGNAL: SPEED (PPS): 12
ADJUST SEND SIGNAL: %BRK: 60
ADJUST SEND SIGNAL: SF FREQ: 1

7.7 SF Adjustments

7.7.01 Engage the following push buttons:

REC INTERFACE: SF, FROM LINE
SF: TWD LINE: OFF HOOK & PULSE
SF: TWD EQUIP: OFF HOOK & PULSE
SEND INTERFACE: TWD LINE, SF

7.7.02 Establish the test set-up of Figure 7-1.

7.7.03 SF Generator Adjustments

1. Adjust ~~C3~~ C14 (OSCILLATOR ADJ) of the MPU (A25) for 2600.0 ±.5Hz on the frequency counter.
2. Adjust the SF FREQ thumbwheel to frequency "2" and check for 3400 Hz ±1 Hz.
3. Adjust the SF FREQ to frequency "3" and check for 3825 Hz ±1 Hz.
4. Adjust R55 (SF SEND LEVEL ADJ) of the SF SEND/RECEIVE DETECTORS (A27) for 1.90Vrms on the ac voltmeter.
5. Terminate the T222C output with a precision 900 ohm resistor.
6. Adjust R4 (TO LINE IMPEDANCE ADJ) of the LEAK CONDITIONS & SF IMPEDANCE (A9) for .95Vrms on the ac voltmeter.
7. Repeat steps 4 through 6 until no adjustment is necessary.
8. Remove the plug from the SF:TO LINE jack and insert it in the SF:TO EQUIP jack.
9. Engage the SEND INTERFACE:TWD DROP/EQ pushbutton. With the precision 900 ohm resistor removed, the ac voltmeter should read 1.90Vrms.
10. Terminate the T222C output with a precision 900 ohm resistor.
11. Adjust R11 (TO EQUIP IMPEDANCE ADJ) of A9 for .95Vrms on the ac voltmeter.

7.7.04 Establish the test set-up of Figure 7-2

7.7.05 SF Receive Adjsutments

1. Common Mode Null Adjustment:
   a. Connect the point marked 1 to the points marked T&R. Connect the point marked 2 to the T222C chassis ground.

b. Adjust the external signal generator for 1.90Vrms at 2600 Hz as read on the ac voltmeter and frequency counter.
c. Using an oscilloscope, monitor the signal at U2 pin 1 of the SF SEND/RECEIVE DETECTORS (A27).
d. Adjust R3 (COMMON MODE NULL ADJ) of A27 for the smallest signal level observed on the oscilloscope.
e. REC INTERFACE, engage:FROM LINE push button; SEND INTERFACE, engage:TWD LINE push button. Connect corresponding SF jacks together. Adjust R47 for REC ON HK lamp to be on from 0 to 26 dB and off at -27 dB.

2. SF Receive Level Adjustments:
a. Connect the points marked 1 and 2 (Figure 7-2) to the points marked T & R respectively.
b. Adjust the external signal generator for .95Vrms at 2600 Hz as read on the ac voltmeter and frequency counter.
c. Remove the 10.0K resistor (R10) on the A/D CONVERTER & FREQUENCY DIVIDER (A26).
d. Insert a 10.0K, 1% resistor from TP1 to TP2 of A26. Using a dc voltmeter, monitor the voltage at TP2.

NOTE: Use the ground reference ON A26 for steps d - h.

e. Adjust R13 (OFFSET ADJUST #1) for 0±1mV as read on the dc voltmeter.
f. Remove the 10.0K resistor between TP1 and TP2. Insert a 12.1K, 1% resistor from TP1 to TP3.
g. Connect the dc voltmeter to TP4, adjust R14 (OFFSET ADJUST #2) for 0±3mv.
h. Remove the 12.1K resistor between TP1 and TP2. Solder the 10.0K, 1% resistor R10 in place.
i. Adjust the external signal generator for .85Vrms. Adjust R1 (REFERENCE ADJUST) for -1dBm on the T222C front panel display.
j. Adjust the external signal generator for 30mVrms. Adjust R12 (SCALE ADJUST) for -30 dBm on the T222C front panel display.
k. Repeat steps i and j until no adjustment is necessary.

7.8 IDT Check

7.8.01 Dismantle test set-up of Figure 7-2 and set the ADJUST SEND SIGNAL thumbwheel switches as described in Section 7.6.02.

7.8.02 Engage the following panel controls:

1. DISPLAY CONTROL: MODE/MEAS/PULSE GEN.
2. DISPLAY CONTROL: FUNCTION/DIALED NUMBER.
3. INTERDIGIT TIME (MS) 700 (three push buttons).

7.8.03 Pulse any digit, press clear and engage repeat "#" on keyboard.

1. Allow 17 digits to be displayed.
2. Engage MODE/PULSE DATA/IDT push button to verify interdigit time of 700 ms.
3. Sixteen interdigit times will be displayed. Each IDT can be verified by repeating step 1.

7.9 Number Storage Check

1. Set the ADJUST SEND SIGNAL thumbwheel switches as per Section 7.6.02.
2. Engage the STORE "*" push button for two seconds if not in STORE mode.
3. Record and enter 16 random digits on the keyboard.
4. Engage DISPLAY CONTROL: MODE/MEAS/PULSE GEN. and FUNCTION/ DIALED NUMBER push buttons.
5. Press the SEND "#" key on the keyboard.
6. After outpulsing all 16 digits, the display will show the digits that were stored.
7. Repeat several times using different groups of 16 digits.

7.10 Loop

7.10.01 On Hook Bias Adjustments

1. Engage SEND INTERFACE:LOOP and REC INTERFACE:LOOP, 'A'RLY.
2. Using a dc voltmeter, measure the voltage at U1 pin 1 of the LOOP DETECTOR (A18).
3. Adjust R5 (GND ON HOOK BIAS ADJ) of A18 for -11.4V on the dc voltmeter.
4. Measure the voltage at U1 pin 7 of A18.
5. Adjust R19 (BATT ON HOOK BIAS ADJ) of A18 for -11.4V on the dc voltmeter.

7.10.02 Loop Receive Adjustment

1. Establish the INITIAL CONDITIONS of Section 7.6.
2. Engage DISPLAY CONTROL: MODE: MEAS: PULSE GEN SEND CONTROL: TRAIN
3. Press a digit (1 through 0) to start the pulse generator.
4. The T222C display should read 60.0 %BK 12.0 PPS.
5. Engage DISPLAY CONTROL: MODE: MEAS: REC. Release LEAK COND:OUT.
6. Uisng a 310 Patch Cord, connect the LOOP:SEND jack to the LOOP:TERM REC jack.
7. Adjust R29 (LOOP RECEIVE ADJ) of the LOOP DETECTOR (A18) for a reading of 60.0 %BK 12.0 PPS on the T222C display.

7.10.03 Bridge Loop Receive Adjustment

1. Establish the test set-up of Figure 7-3.
2. Short the points marked 1 and 2 together.
3. Adjust R47 (BRIDGING LOOP RECEIVER ADJ) of A18 so that the REC ON HK lamp just turns off.

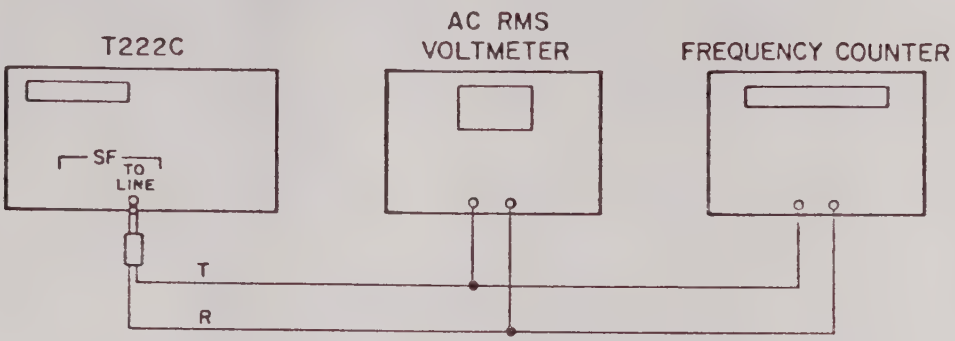


FIGURE 7-1

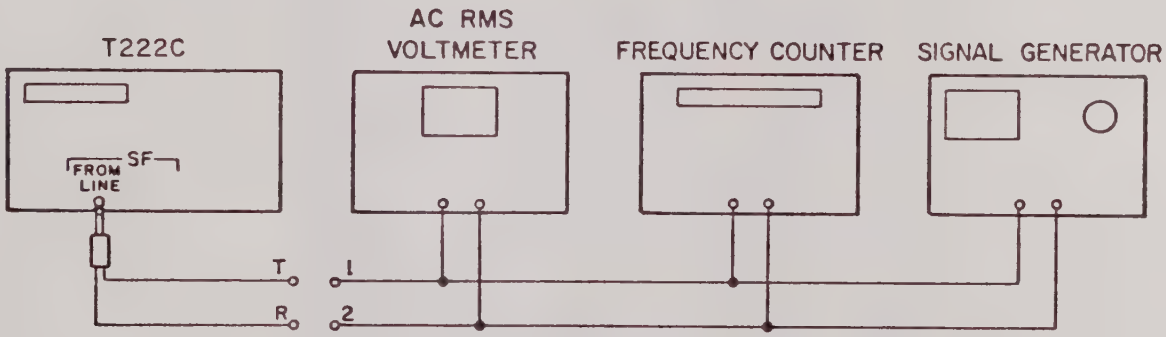
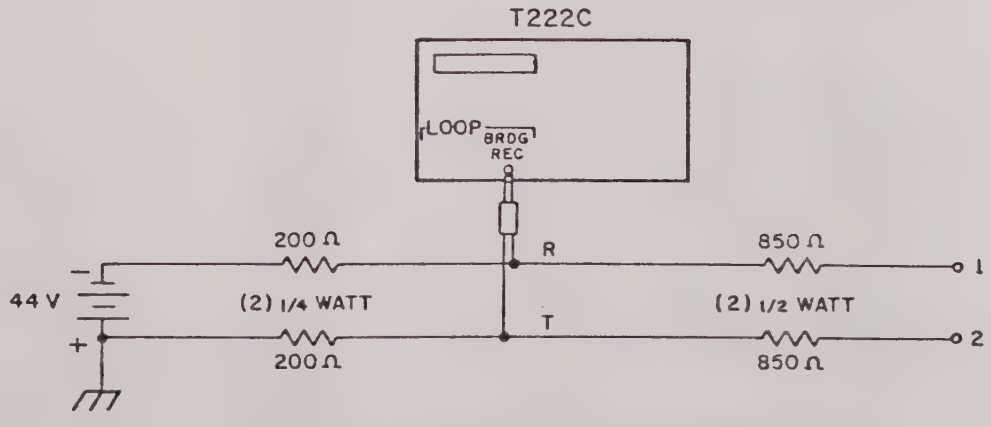


FIGURE 7-2



NOTE: CONNECT +BATT TO T222C CHASSIS GROUND.

FIGURE 7-3

7.11 Printed Circuit Assembly Removal - Removal instructions follow the sequence used for the Circuit Descriptions of Section 6.0. Be sure the ac power cord is removed from the test set when an assembly is being removed or replaced. Use reasonable care when removing or replacing PC assembly plugs. Refer to figures 7-4, 7-5 & 7-6.

7.11.01 Outpulsing Circuits

1. Rate % Break Generator, A21, removal. Refer to Section 7.3.05.
2. Interdigit Time Select, A29, removal -
    a. Remove plug from P.C. assembly.
    b. Remove two screws from the front panel above and below INTERDIGIT TIME push buttons.
    c. Carefully remove PC-push-button assembly as a unit.
3. Keyboard-Decoder-Store Control, A30. Remove as per Section 7.3.05.
4. Keyboard and SF Attenuator, A15, removal -
    a. Remove plugs from P.C. assembly.
    b. Remove four screws from the front panel - two on each side of keyboard.
    c. Remove keyboard assembly using care not to bend LEDs out of position.
5. Loop Resistance and Send Control, A8, removal -
    a. Remove plugs from P.C. assembly.
    b. Remove screw from each side of ADD LOOP RESISTANCE and SEND CONTROL push buttons on the front panel.
    c. Remove plug from assembly A9 (beneath the assembly being removed).
    d. Carefully remove PC-push-button assembly A8.
    e. Replace plug to assembly A9.

7.11.02 Self Scan Display

1. Display Control Switching, A10, removal -
    a. Unplug the end of assembly A10 and unplug the four plugs on the two vertically mounted assemblies beneath this plug.
    b. Unplug the green plug on the Display Assembly.
    c. Remove PC assembly A29 - see Section 7.11.01 #2.
    d. Remove front panel screws - one on each side of DISPLAY CONTROL push buttons. The REC ON HK "LED" may have to be coaxed out of its red plastic cylinder.
    e. Push the PC assembly out of the front panel and slide toward the center. (The two LEDs beneath the assembly may have to be removed.)
2. Interrupt Timer and Self Scan Display, A23, Removal. Refer to Section 7.3.05.
3. 12-250V Converter, A16, removal -
    a. Remove four screws from the side of the main frame while supporting the PC assembly.

7.11.03 Central Processing Unit

1. Data Input Control, A24, removal. Refer to Section 7.3.05.
2. Interrupt Timer and Self Scan Interface, A23, removal. Refer to Section 7.3.05.
3. A/D Converter and Frequency Divider, A26, removal. Refer to Section 7.3.05.
4. CPU, A25, removal. Refer to Section 7.3.05.

7.11.04 SF Analog Digital Interface

1. A/D Converter and Frequency Divider, A26, removal. See Section 7.11.03, #3.
2. SF Send/Receive Detector, A27, removal. Refer to Section 7.3.05.
3. Data Input Control, A24, removal. See Section 7.11.03, #1.
4. SF Attenuator (part of A15) removal. Refer to Section 7.11.01, #4.

7.11.05 Send Interface and Receive Interface Controls

1. Receive Pulsing Type assembly A5 and Send Pulse Type Control assembly A7 are mechanically paired with assemblies A6 and A11 respectively. Removal of either pair is accomplished as follows:
   a. Remove front panel screws from both ends of either push button assembly pair - REC INTERFACE push buttons or SEND INTERFACE push buttons.
   b. Push the pair out of the front panel and rotate upward for easy access.

7.11.06 Loop and Line Pulser Circuits

1. Loop and Line Pulser, assembly A17, removal is accomplished by turning the test set on its side and removing the four screws from the underside of the set. The assembly is then free to be rotated away from the front panel.

7.11.07 Signaling Send/Receive Interface Circuits -

A. The Loop Signaling: Send/Receive Interface Circuits are listed below along with the section describing removal instructions. Following the list are removal instructions not described previously.

ASSEMBLY	SECTION
1. Receive Pulsing Type A5	7.11.05
2. Receive Interface Control A6	7.11.05
3. Send Pulse Type Control A7	7.11.05
4. Loop and Line Pulser A17	7.11.06
5. Send Interface Control A11	7.11.05
6. Loop Resistance & Send Control A8	7.11.01, #5

ASSEMBLY — SECTION

7. Loop Detector, A18, removal -
   a. Remove four screws on side of main frame
8. Leak Conditions (and SF Impedance), A9, removal -
   a. Remove plug from PC assembly.
   b. Remove screw from each side of LEAK COND and SF IMP push buttons on front panel.
   c. Push assembly out of front panel while supporting it from the other side.
9. Beneath the Display Control Switching assembly, A10, are three PC assemblies listed below -
   A12 E&M Supervision
   A13 SF Supervision
   A14 DX Supervision
   On the front panel the overall label for each push button group is E&M, SF or DX. Assembly removal as a group is as follows:
   a. Remove the front panel screws on each side of the three push button assemblies E&M, SF and DX.
   b. It is not necessary to unplug the plugs on these PC assemblies. However, it is obviously necessary to remove the ribbon cables from the adjacent pairs of vertical PC assemblies if attached.
   c. Push all three assemblies out of the front panel as a unit and rotate up for easy access.

B. DX Signaling: Send/Receive Interface
The DX Signaling Send/Receive Interface removal instruction references are listed below -

ASSEMBLY	SECTION
1. DX Supervision A14	7.11.07, A, #9
2. Receive Pulsing Type A5	7.11.05
3. Receive Interface Control A6	7.11.05
4. Send Interface Control A11	7.11.05
5. Loop and Line Pulser A17	7.11.06
6. Send Pulse Type Control A7	7.11.05
7. Loop Resistance and Send Control A8	7.11.01, #5

C. E&M Signaling: Send Receive Interface
The E&M Signaling Interface removal instruction references are shown below -

ASSEMBLY	SECTION
1. Loop and Line Pulser A17	7.11.06
2. E&M Supervision A12	7.11.07, A, #9
3. Send Interface Control A11	7.11.05
4. Receive Interface Control A6	7.11.05

D. The SF Supervision Circuits Assembly, A13, removal is included in Section 7.11.07, A, #9.

7.11.08 Power Supply

1. Power Supply assembly, A19, removal. Most of the power supply terminals can be reached with the rear access panel open. However, if removal is necessary
    a. Remove all plugs
    b. Remove five screws from back of panel.
    c. Gently work assembly away from the panel.

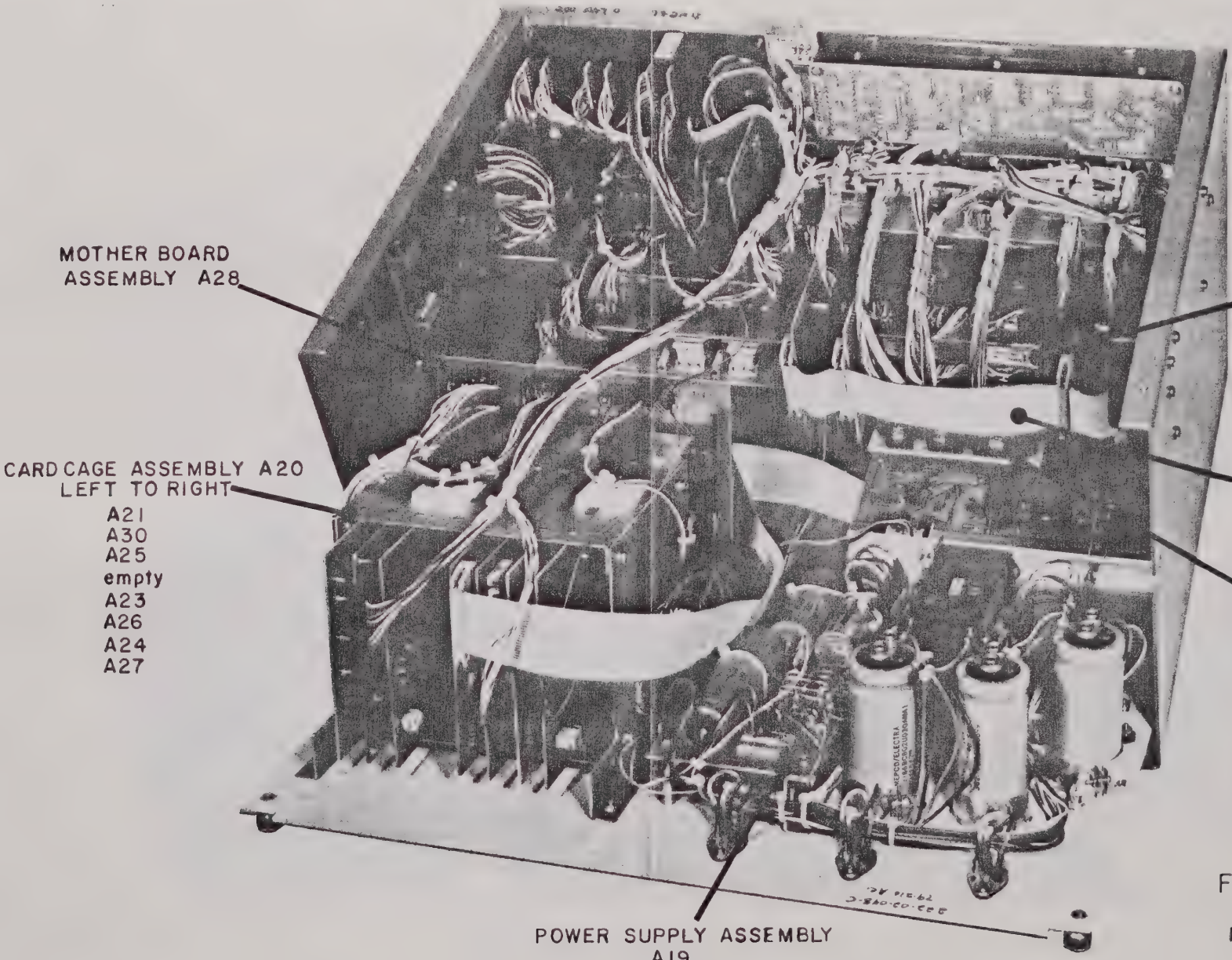


FIGURE 7-4
T 222C
REAR VIEW

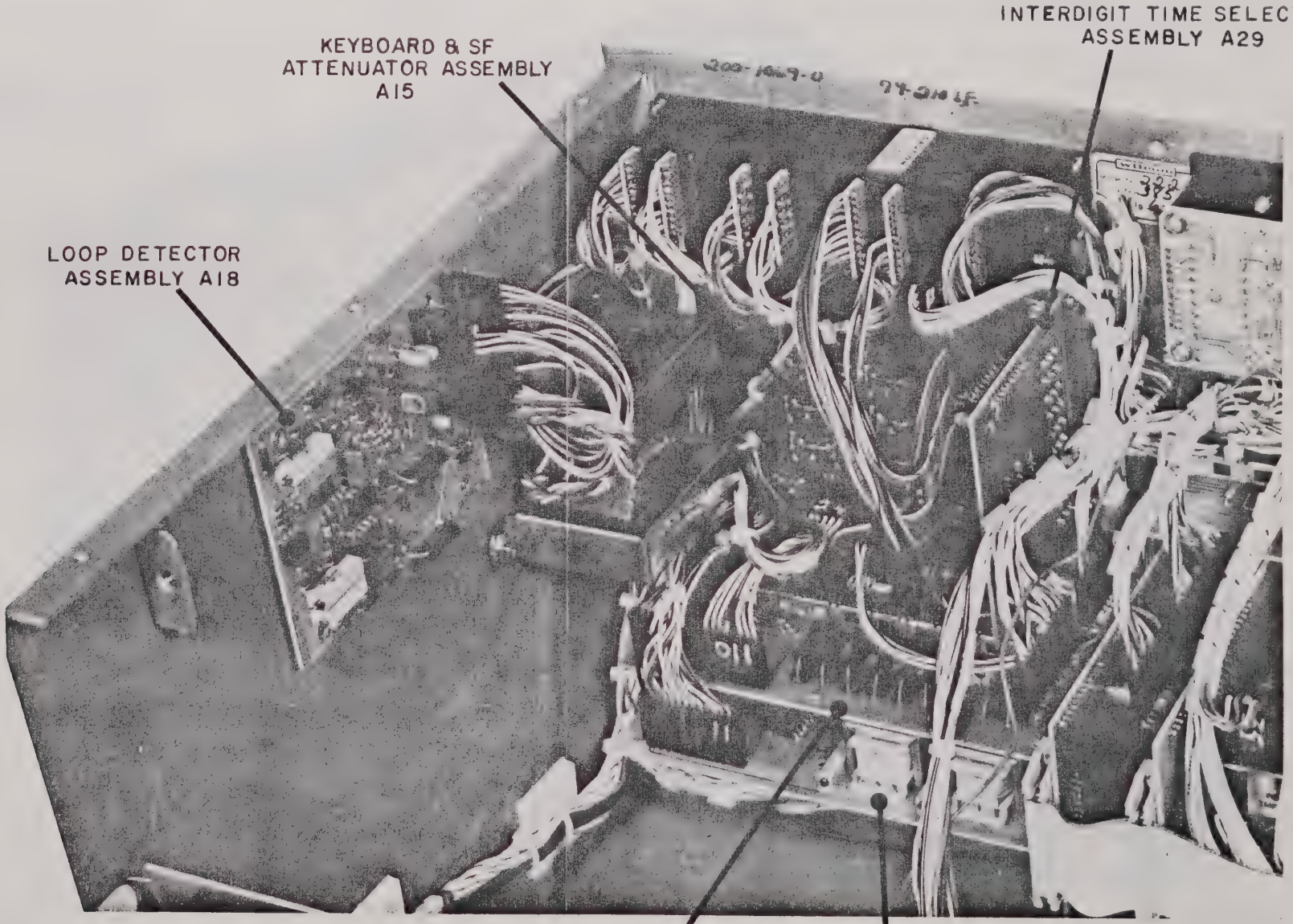


FIGURE 7-5
T222C
LEFT REAR VIEW

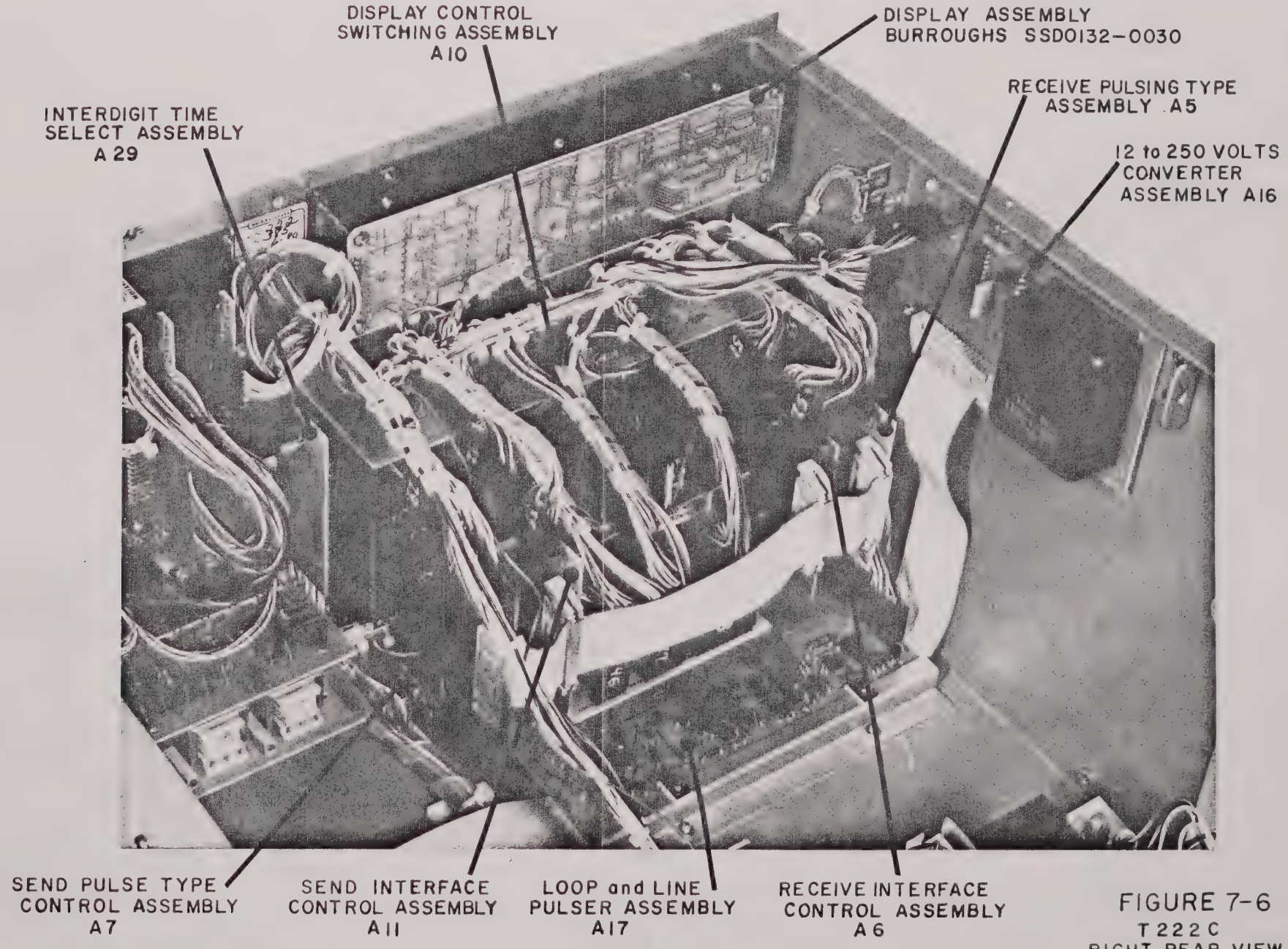


FIGURE 7-6
T 222 C
RIGHT REAR VIEW

8.0 SCHEMATIC AND LAYOUT DRAWINGS

8.1 General

8.1.01 The following pages provide the illustrations useful in locating and identifying the various assemblies that make up the Model T222C Signaling Test Set.

8.1.02 The necessary schematic diagrams and layout drawings of each sub-assembly are given to allow identification of various components, controls and terminals on the circuit boards. This information will be useful to those with the facilities to provide maintenance and calibration of this test equipment.

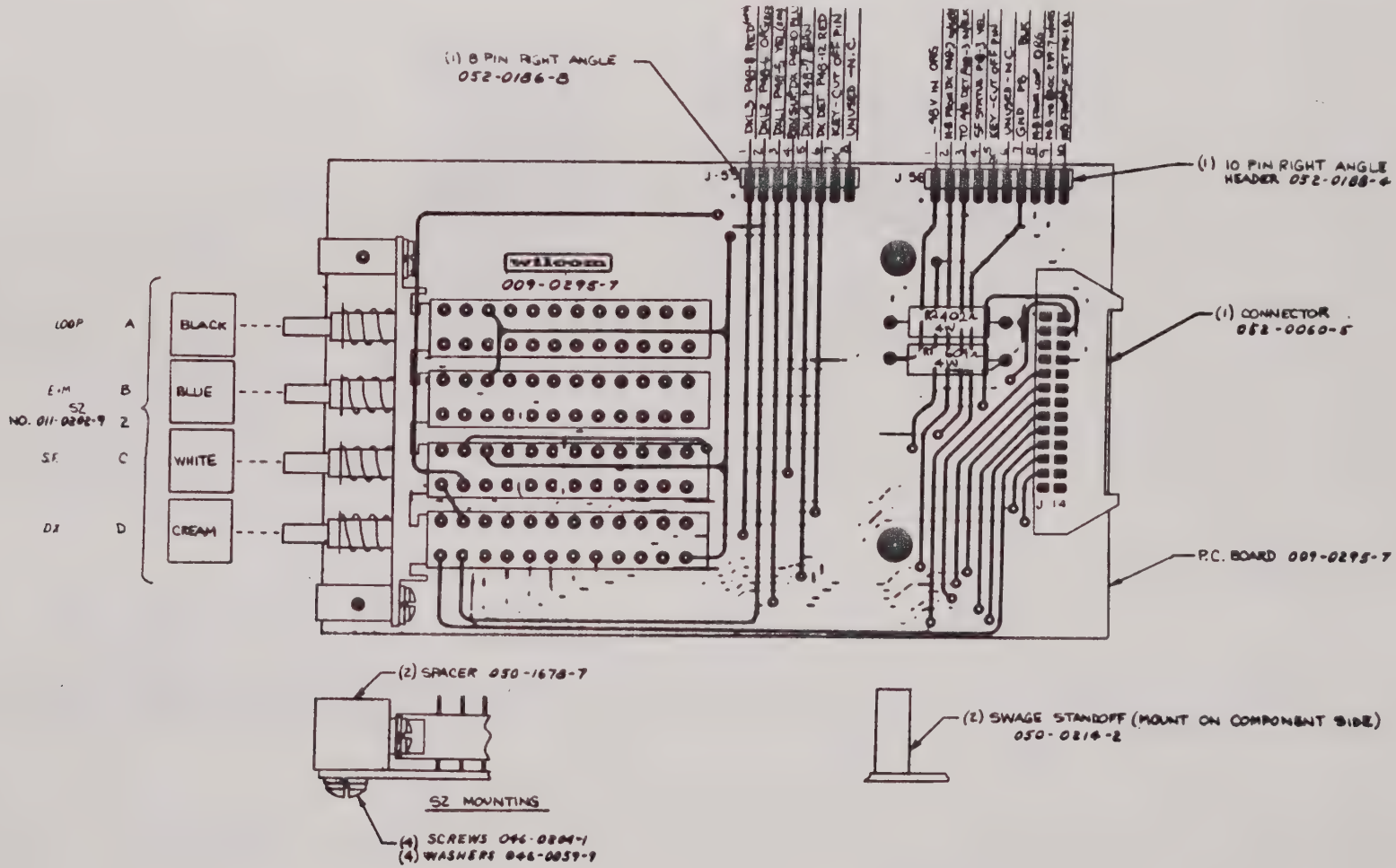


FIGURE 8-1

Receive Pulsing Type

PC Assembly A5

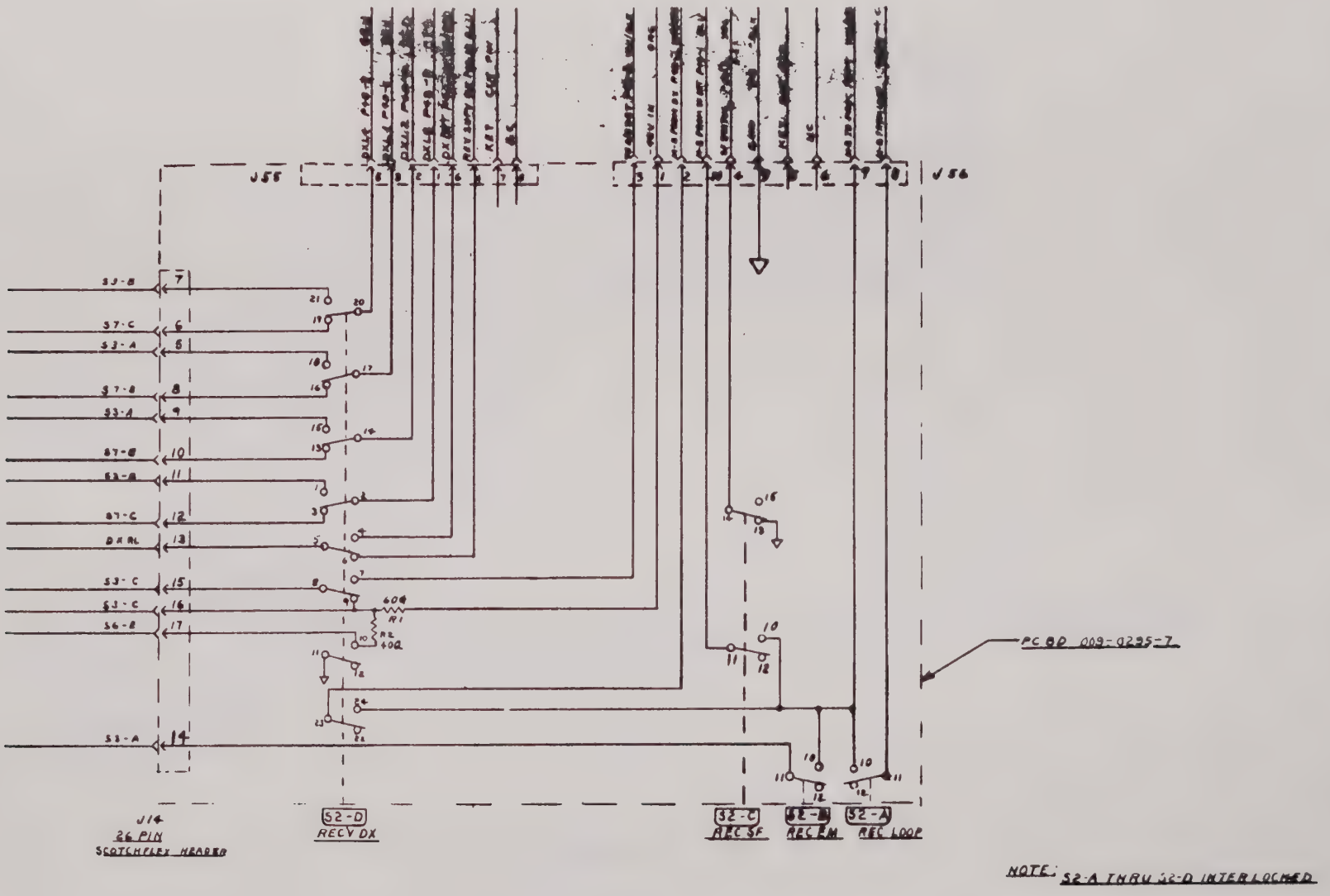


FIGURE 8-2

Recieve Pulsing Type

Schematic A5

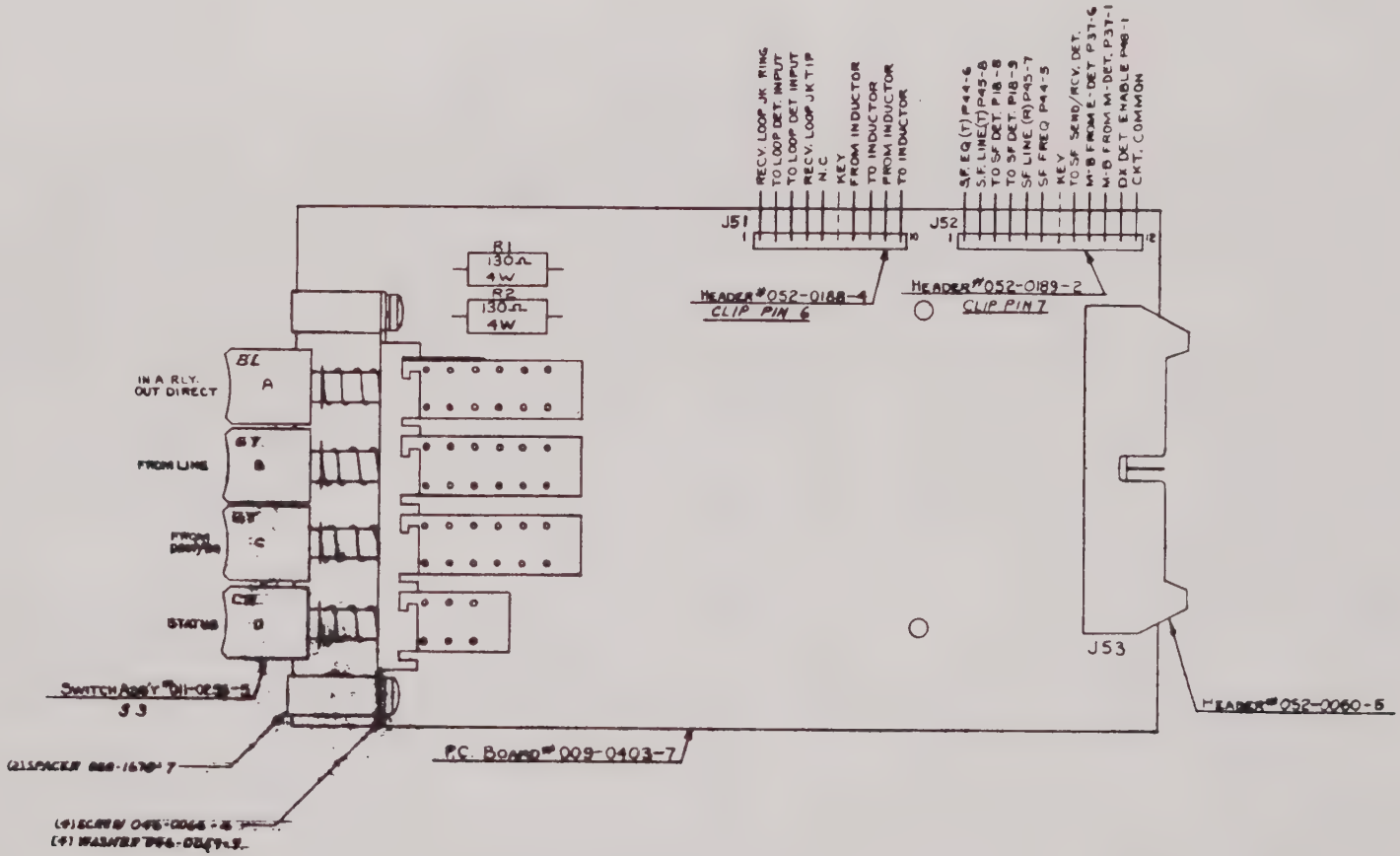


FIGURE 8-3

Recieve Interface Control

PC Assembly A6

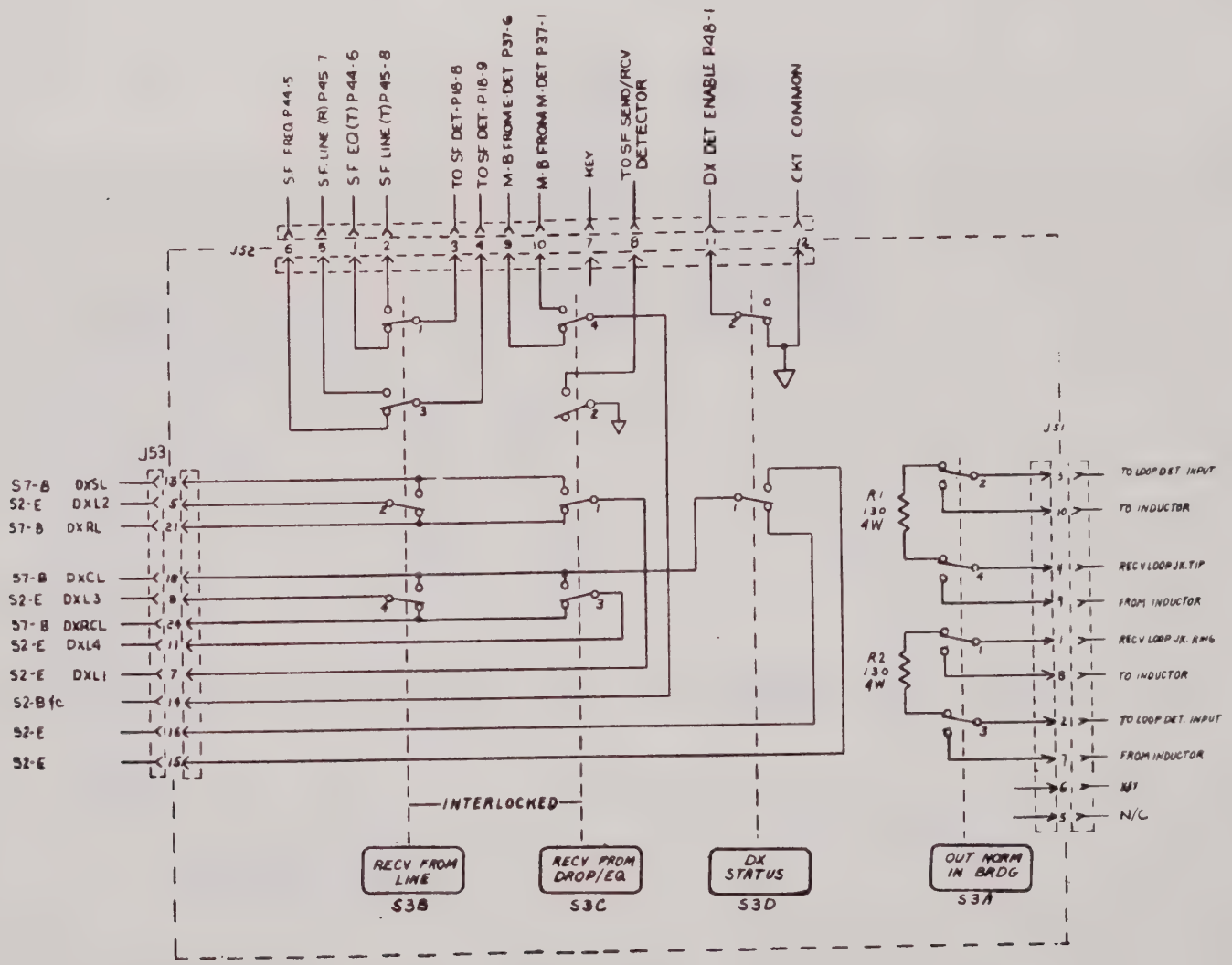


FIGURE 8-4

Receive Interface Control

Schematic A6

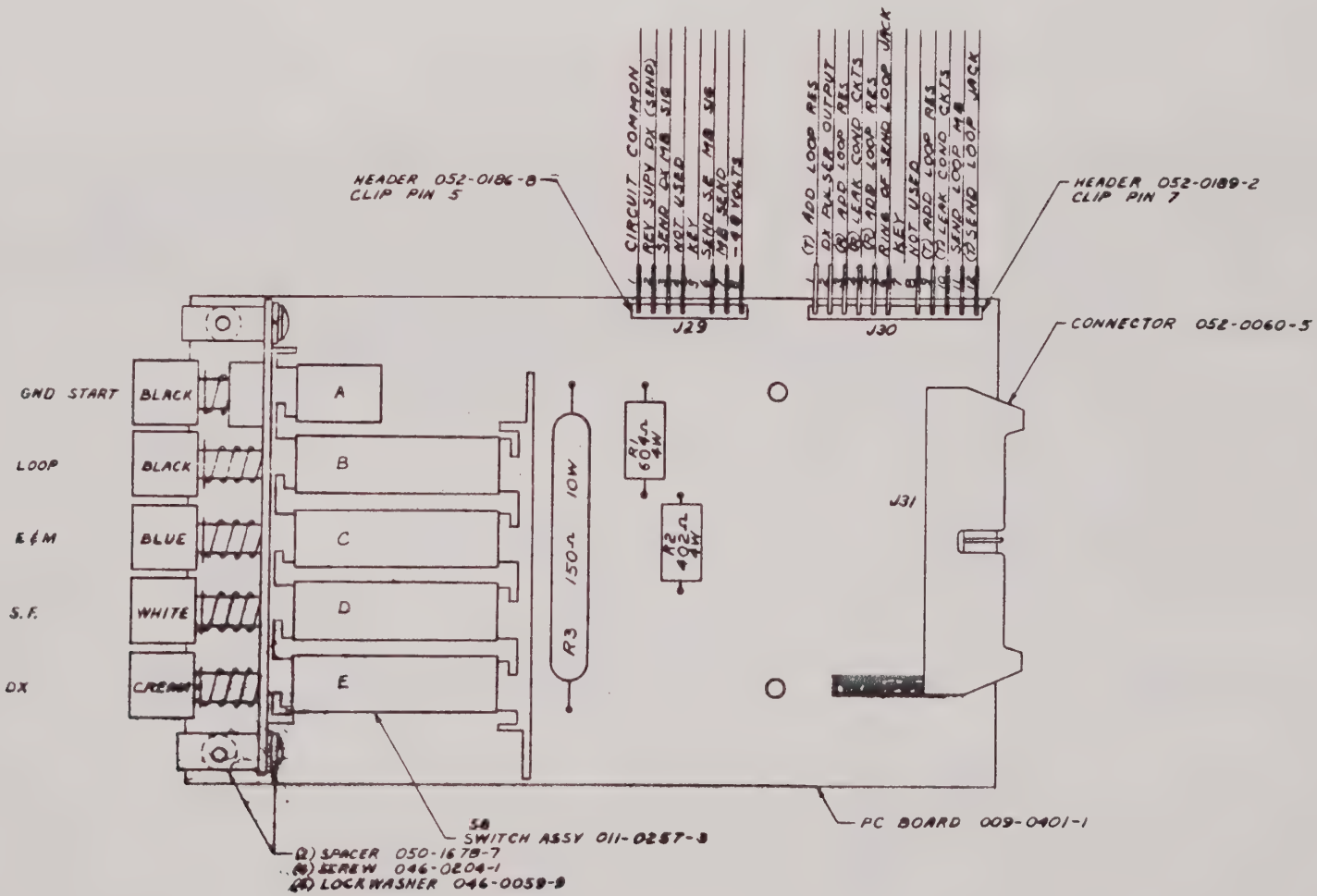
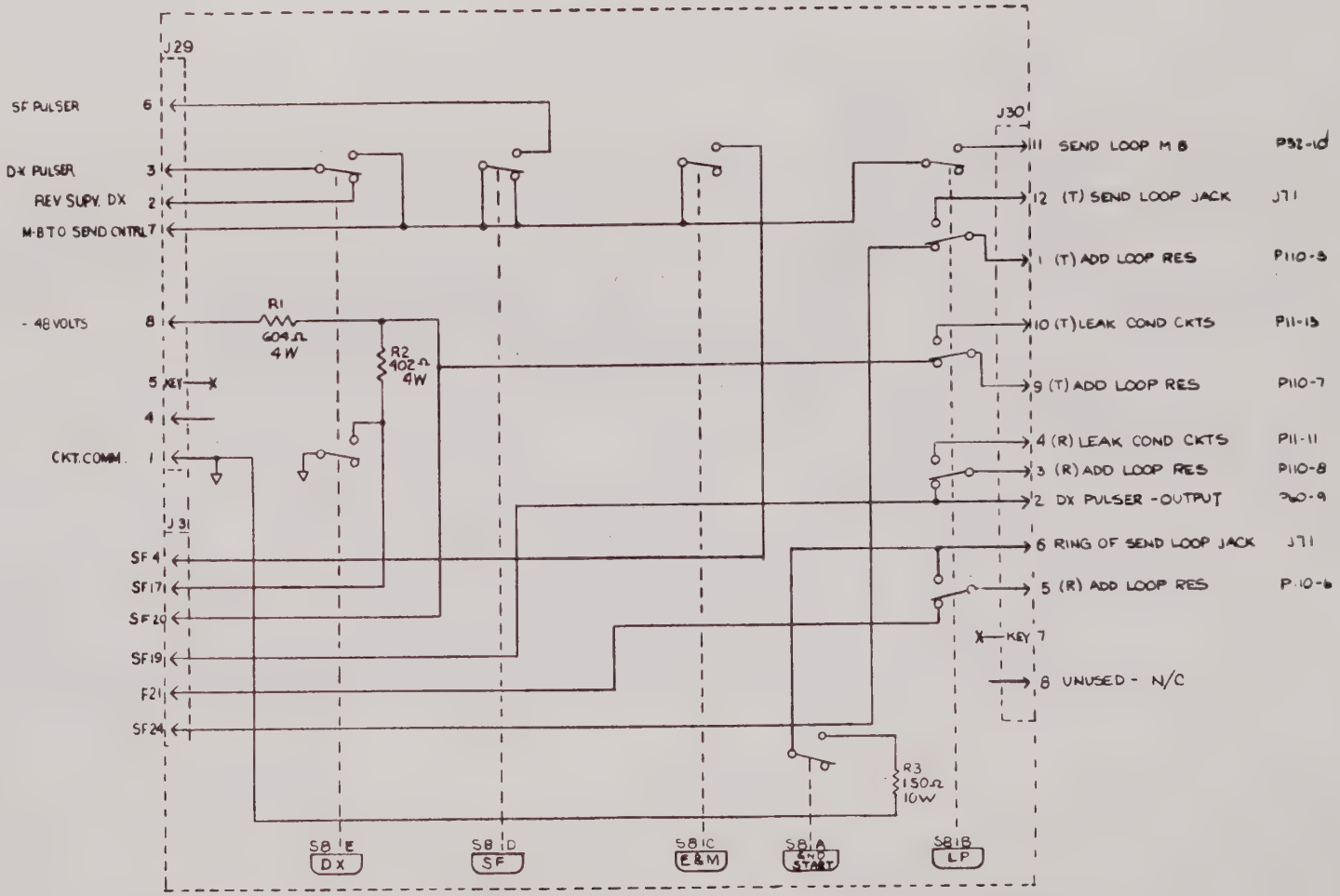


FIGURE 8-5

Send Pulse Type Control

PC Assembly A7



HIGHEST COMPONENT REFERENCE DESIGNATION		
R 3		

FIGURE 8-6

Send Pulse Type Control

Schematic A7

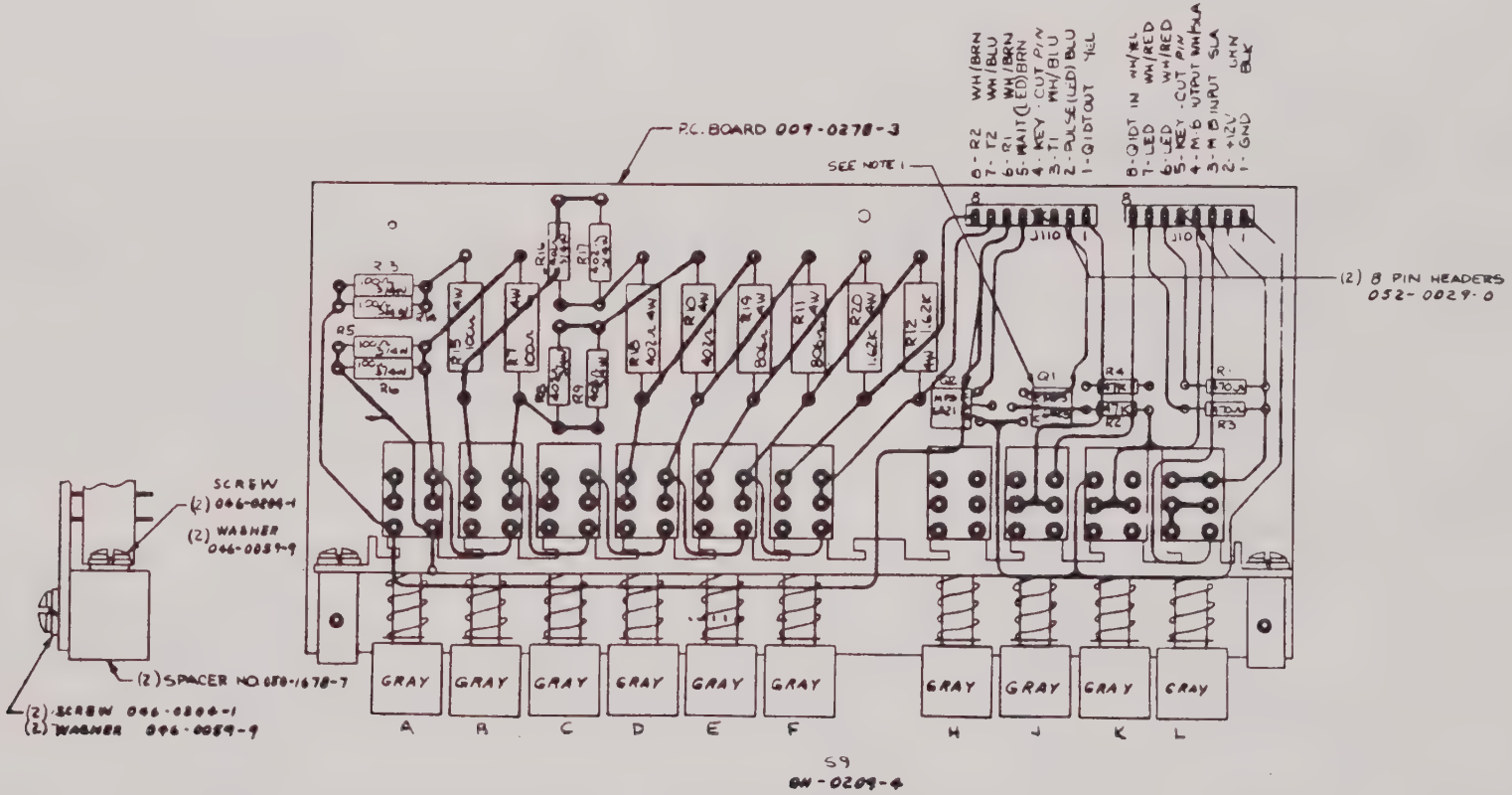


FIGURE 8-7

Loop Resistance and Send Control

PC Assembly A8

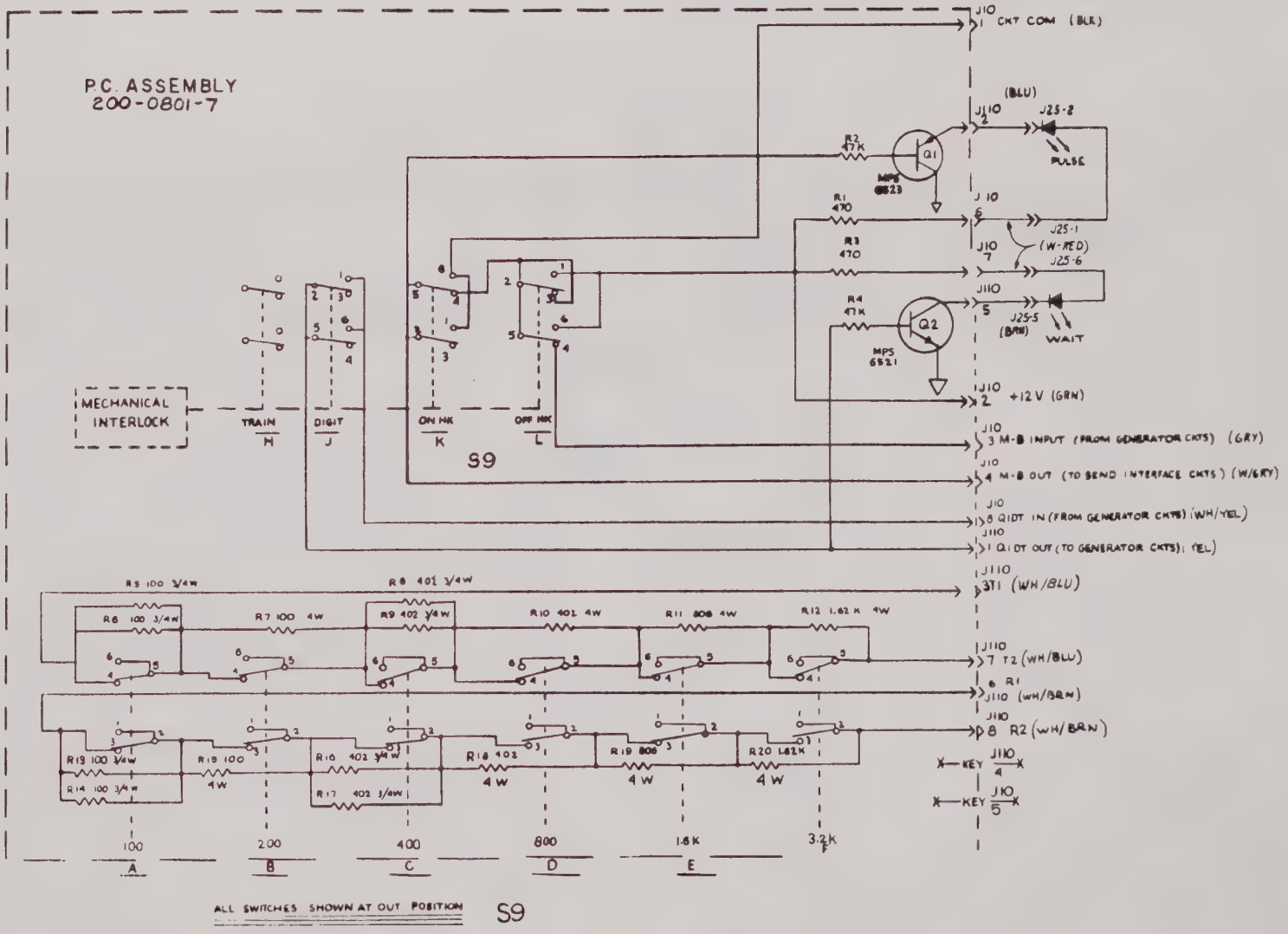
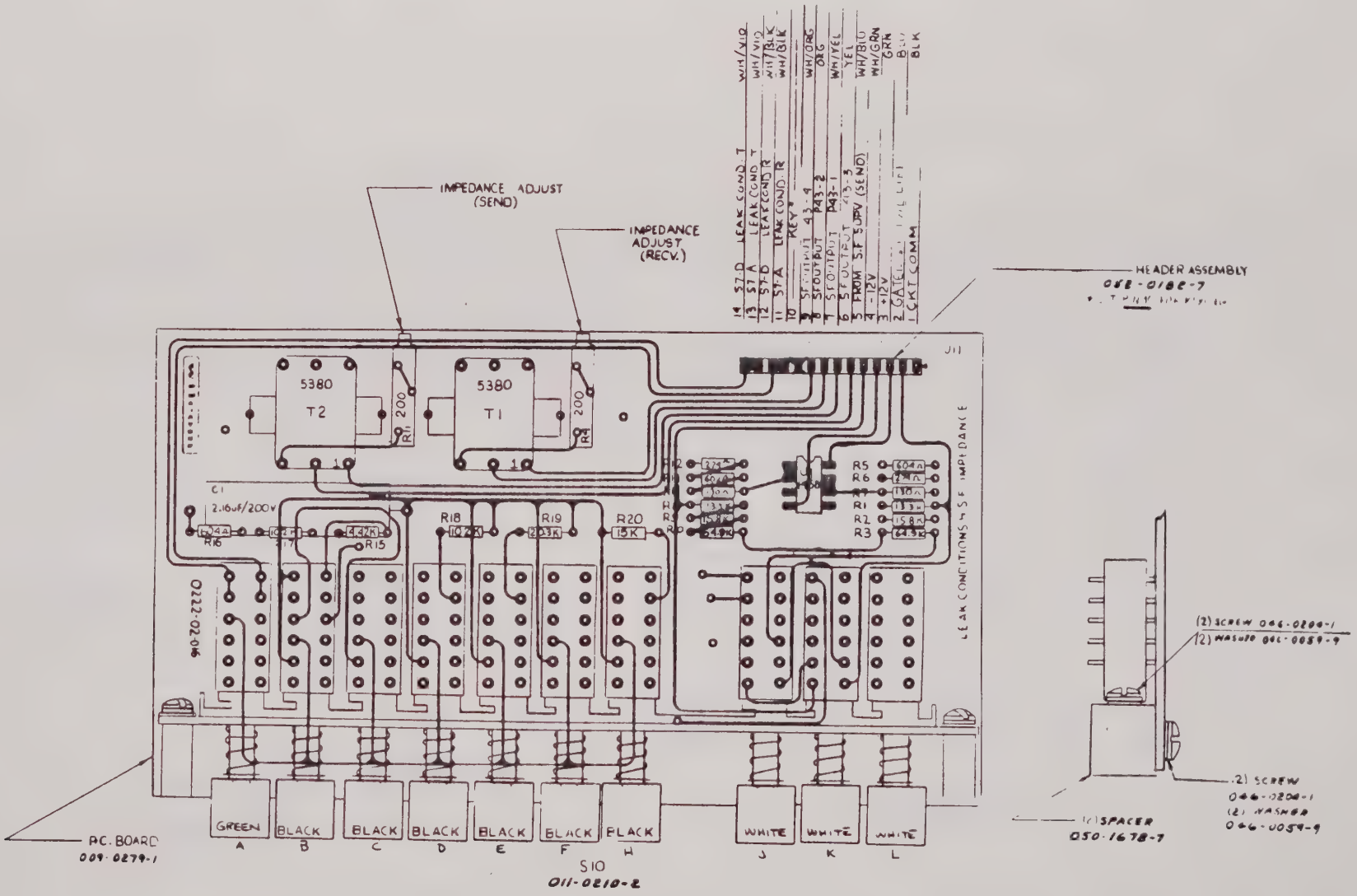


FIGURE 8-8

Loop Resistance and Send Control

Schematic A8

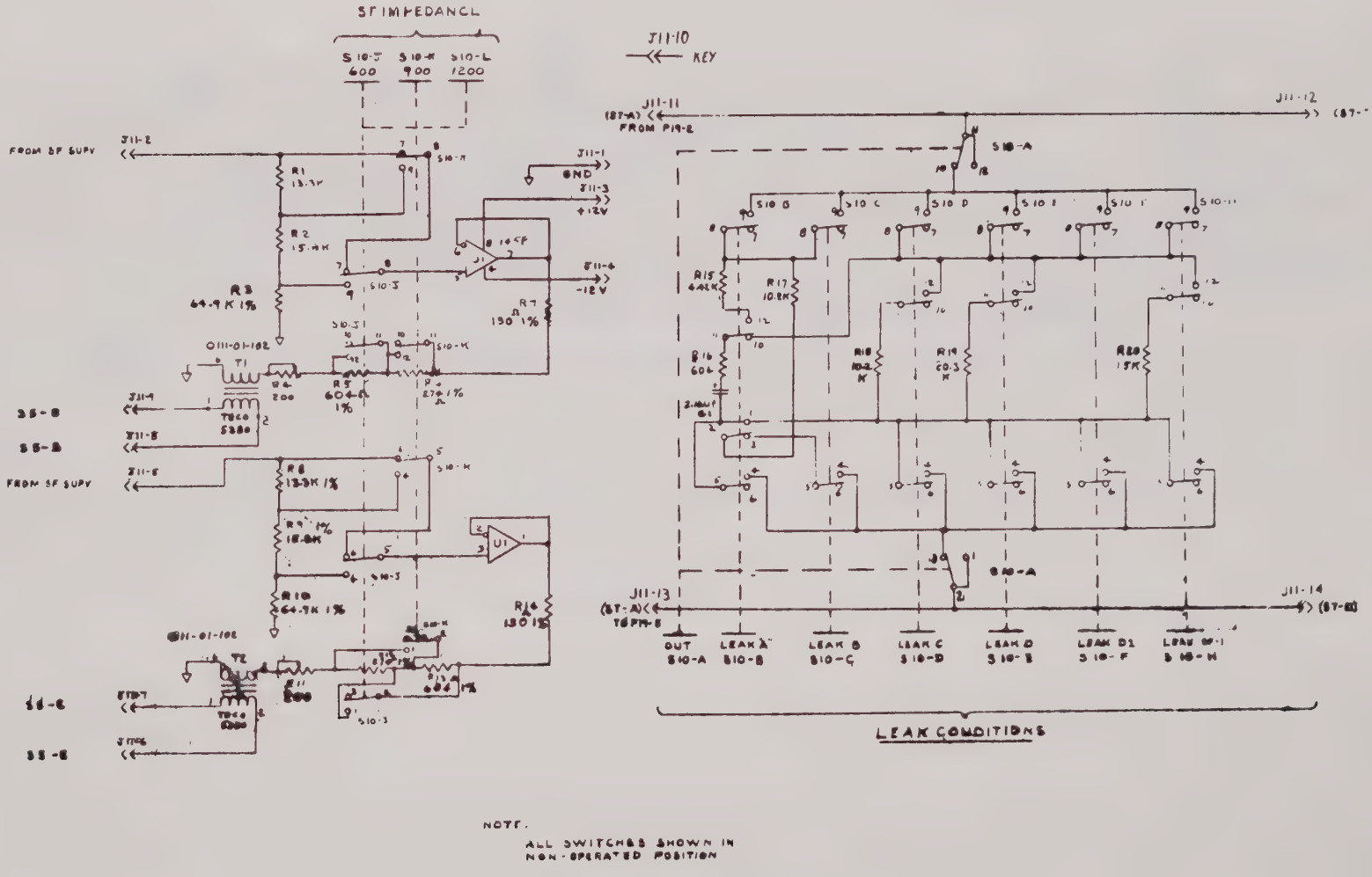


NOTE:
ALL FIXED RESISTORS ±1%.

FIGURE 8-9

Leak Condition and SF Impedance

PC Assembly A9



NOTE:
ALL SWITCHES SHOWN IN NON-OPERATED POSITION

FIGURE 8-10

Leak Conditions and SF Impedance

Schematic A9

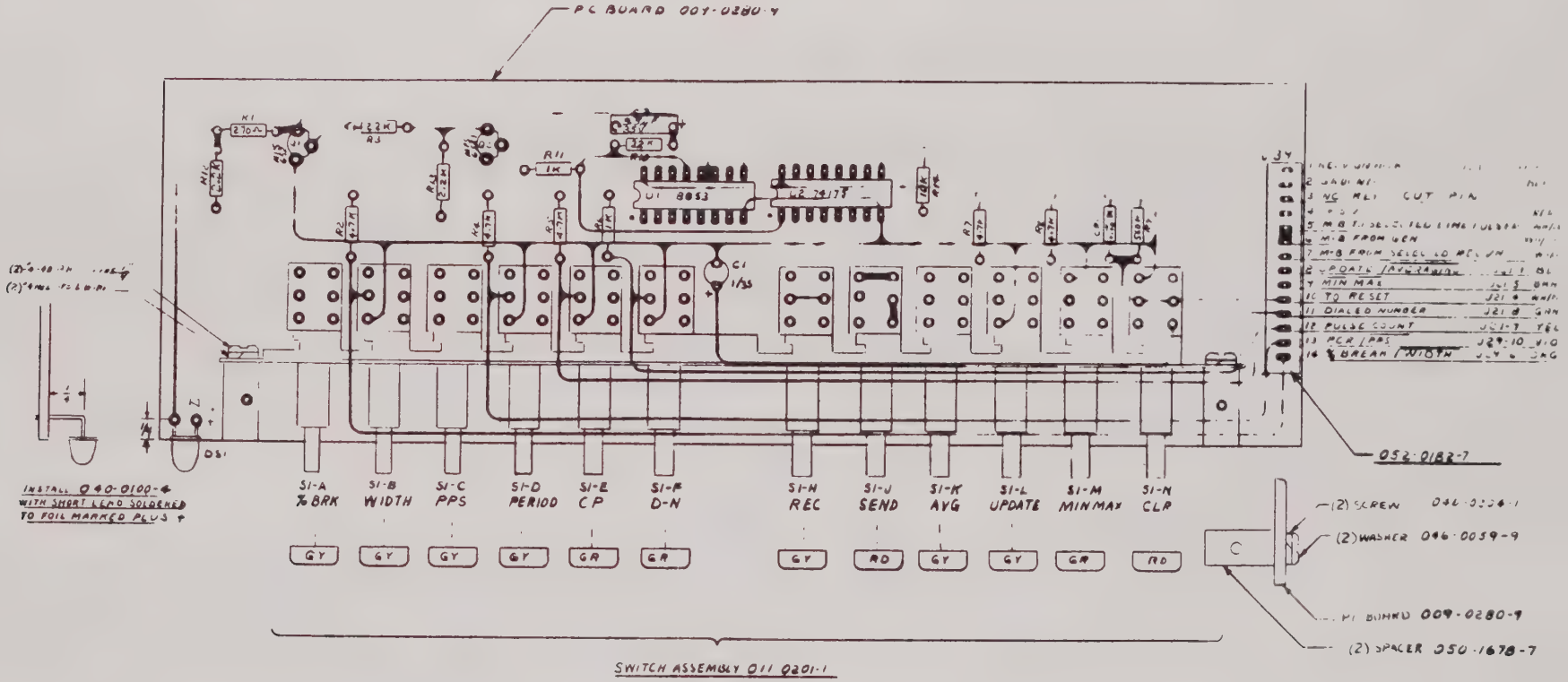


FIGURE 8-11

Display Control Switching

PC Assembly A10

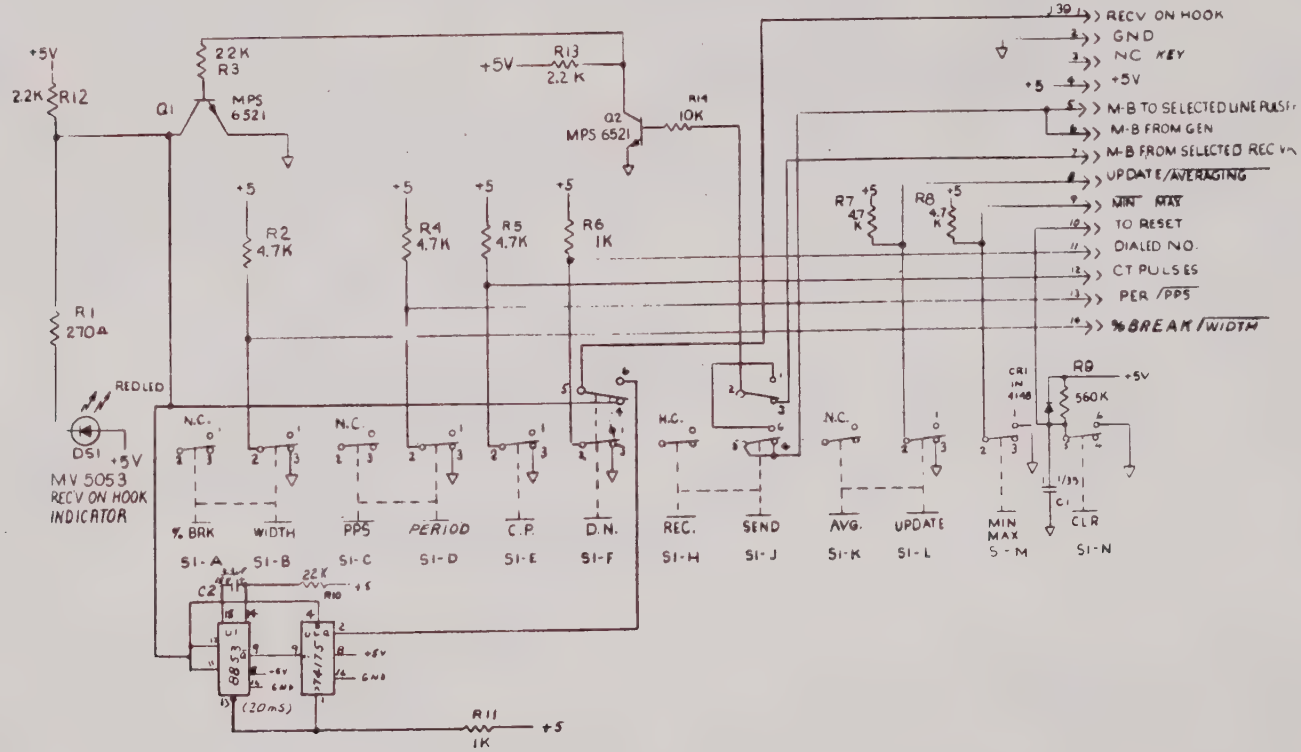


FIGURE 8-12

Display Control Switching

Schematic A10

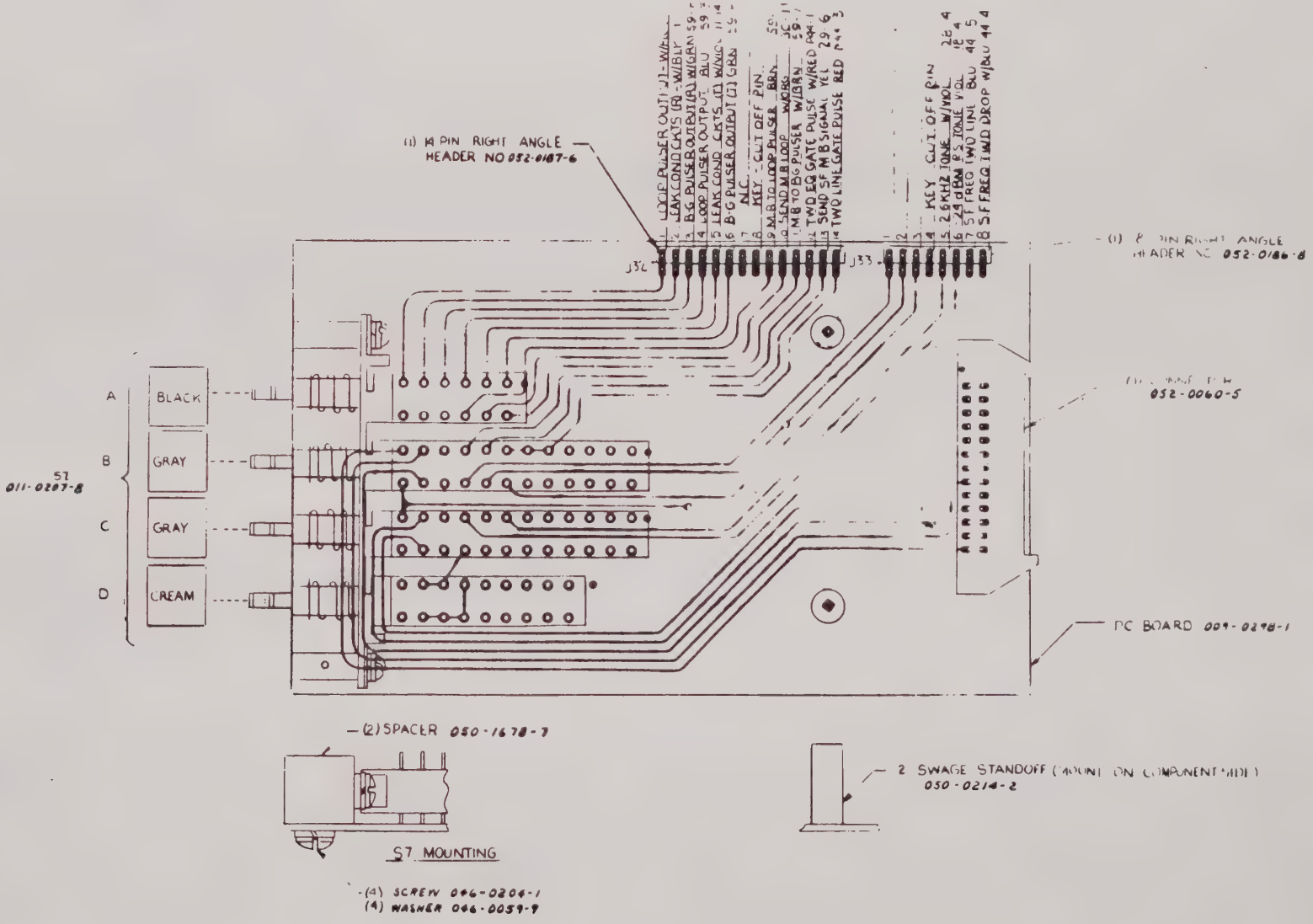


FIGURE 8-13

Send Interface Control

PC Assembly A11

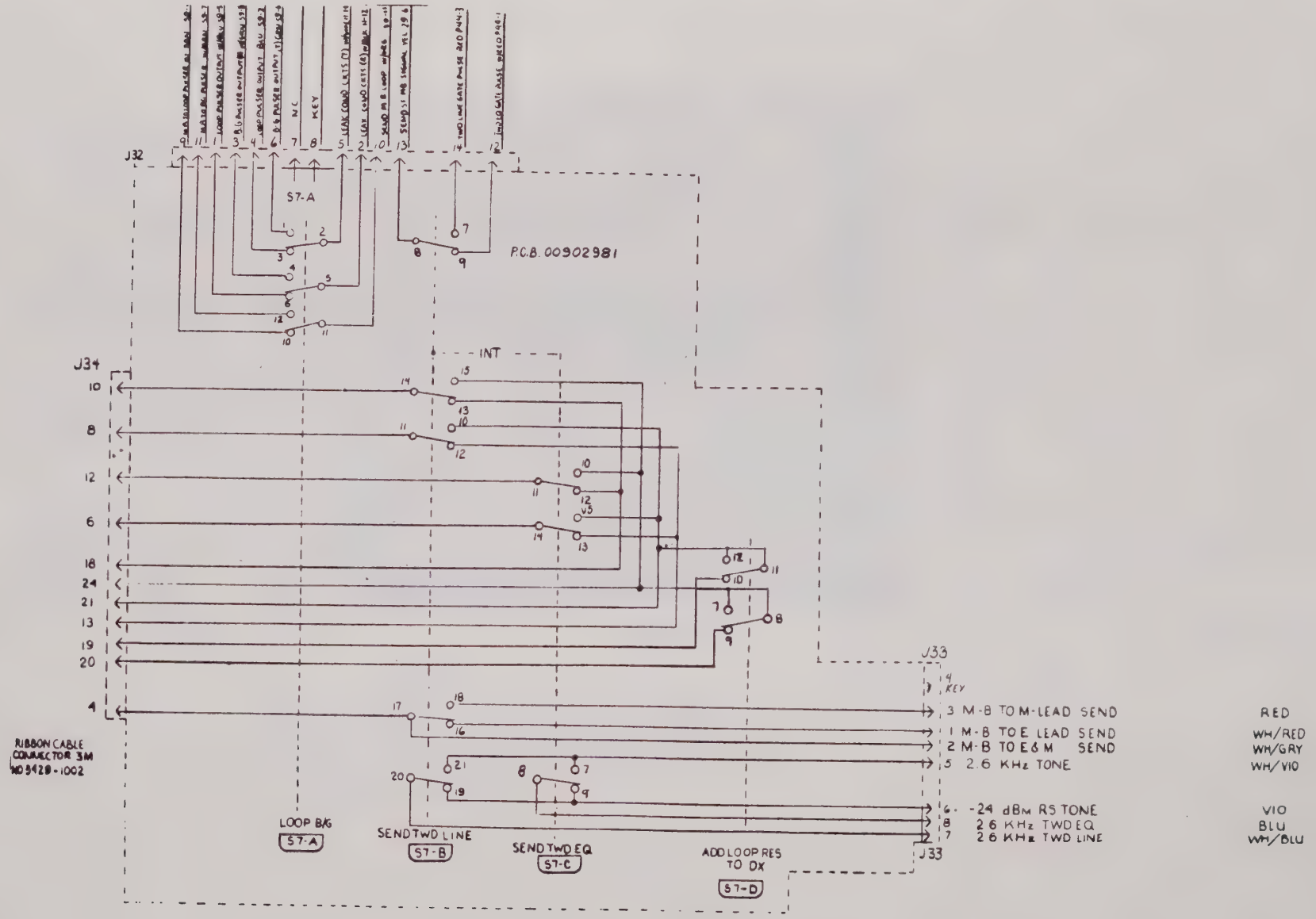


FIGURE 8-14

Send Interface Control

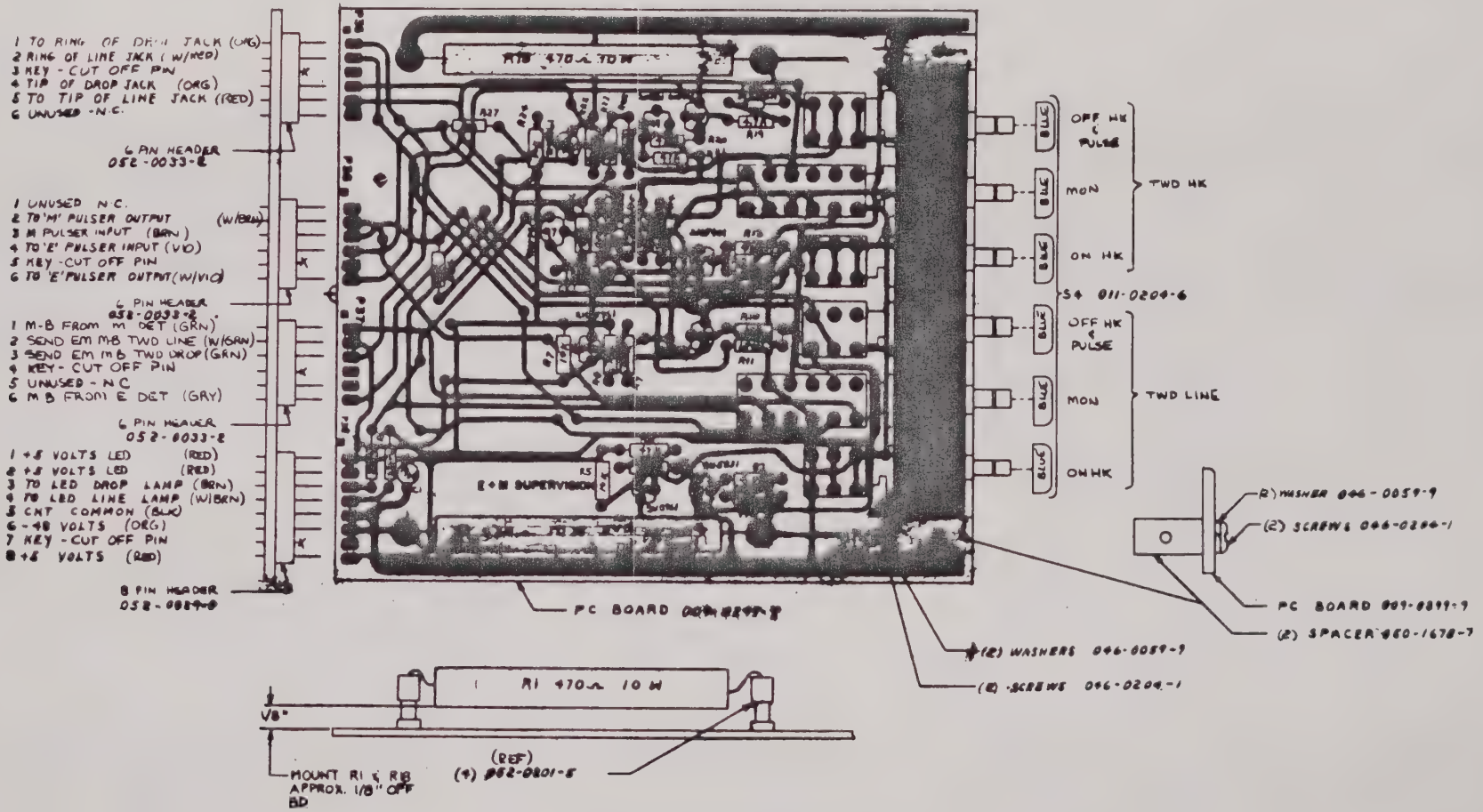


FIGURE 8-15

E & M Supervision

PC Assembly A12

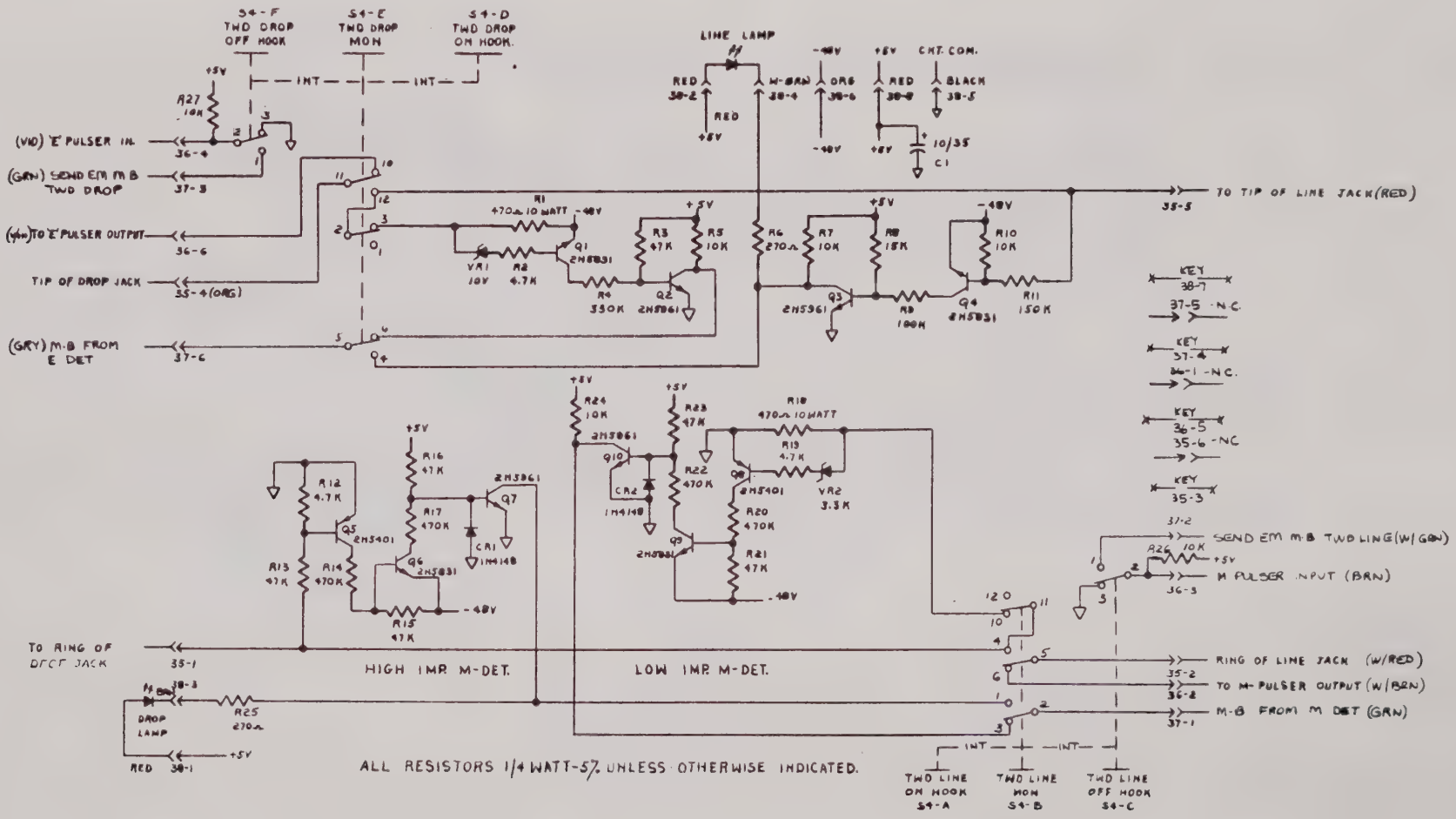


FIGURE 8-16

E & M Supervision

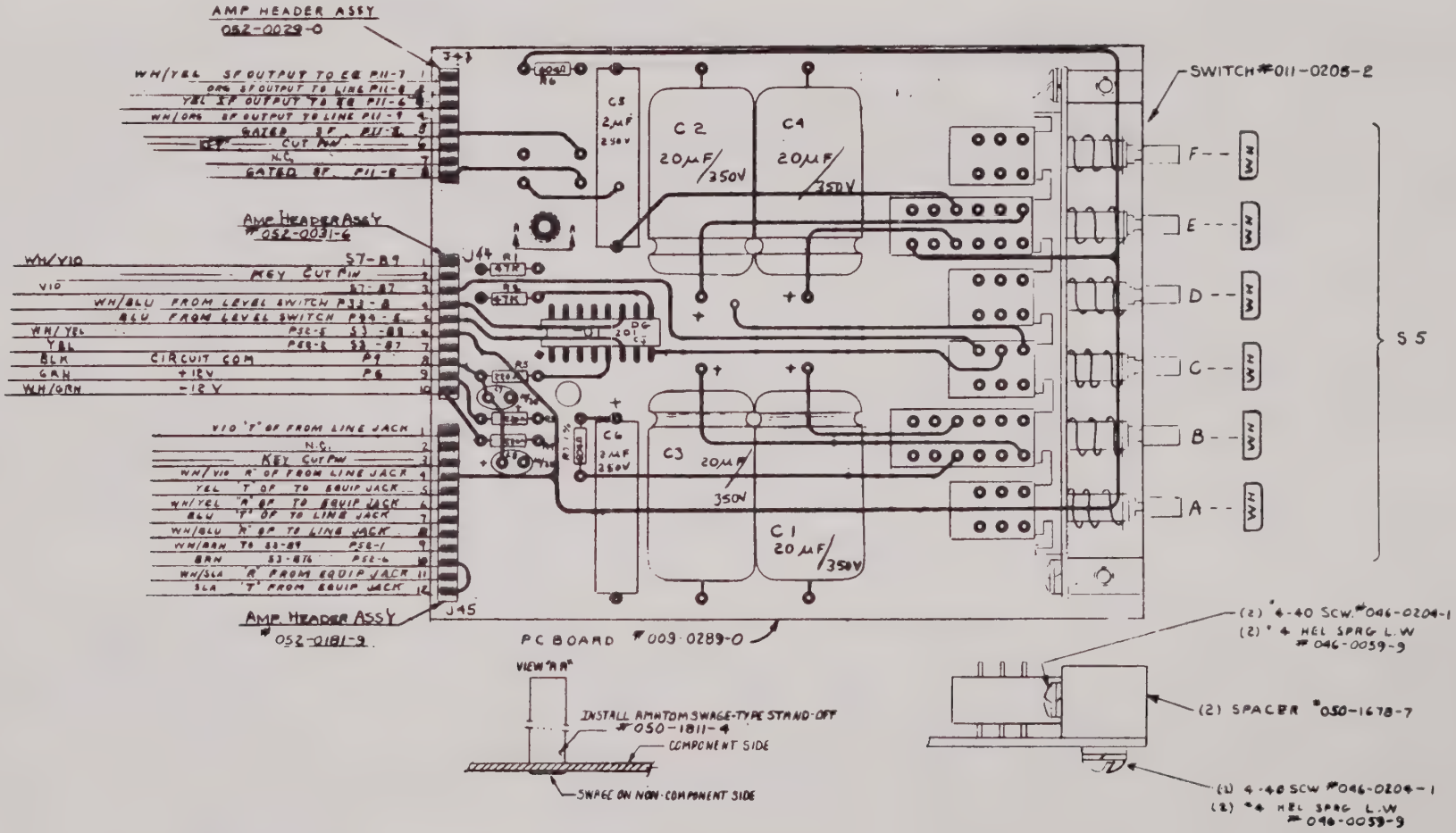
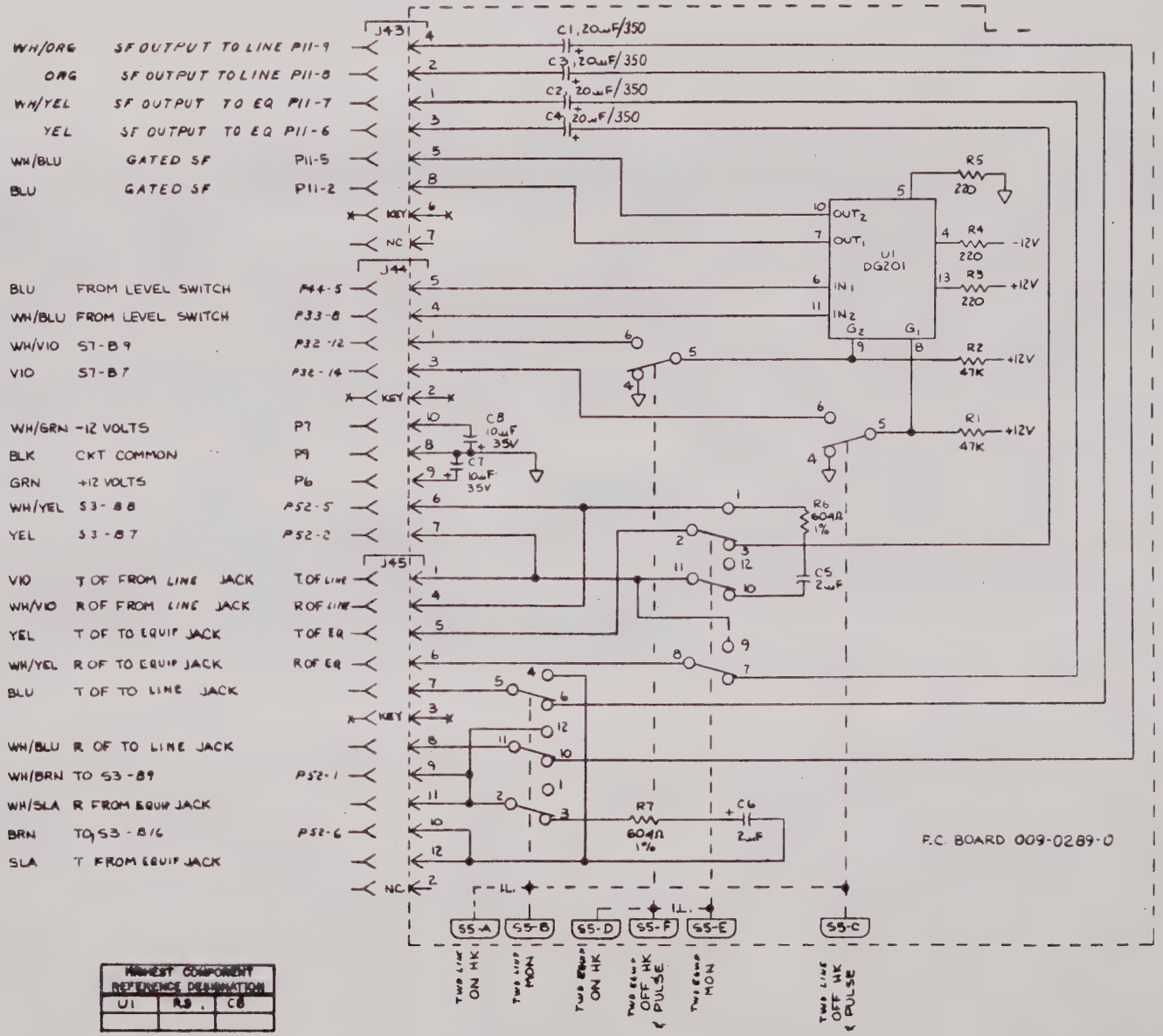


FIGURE 8-17
SF Supervision
PC Assembly A13



HIGHEST COMPONENT REFERENCE DESIGNATION		
U1	R9	C8

FIGURE 8-18
SF Supervision
Schematic A13

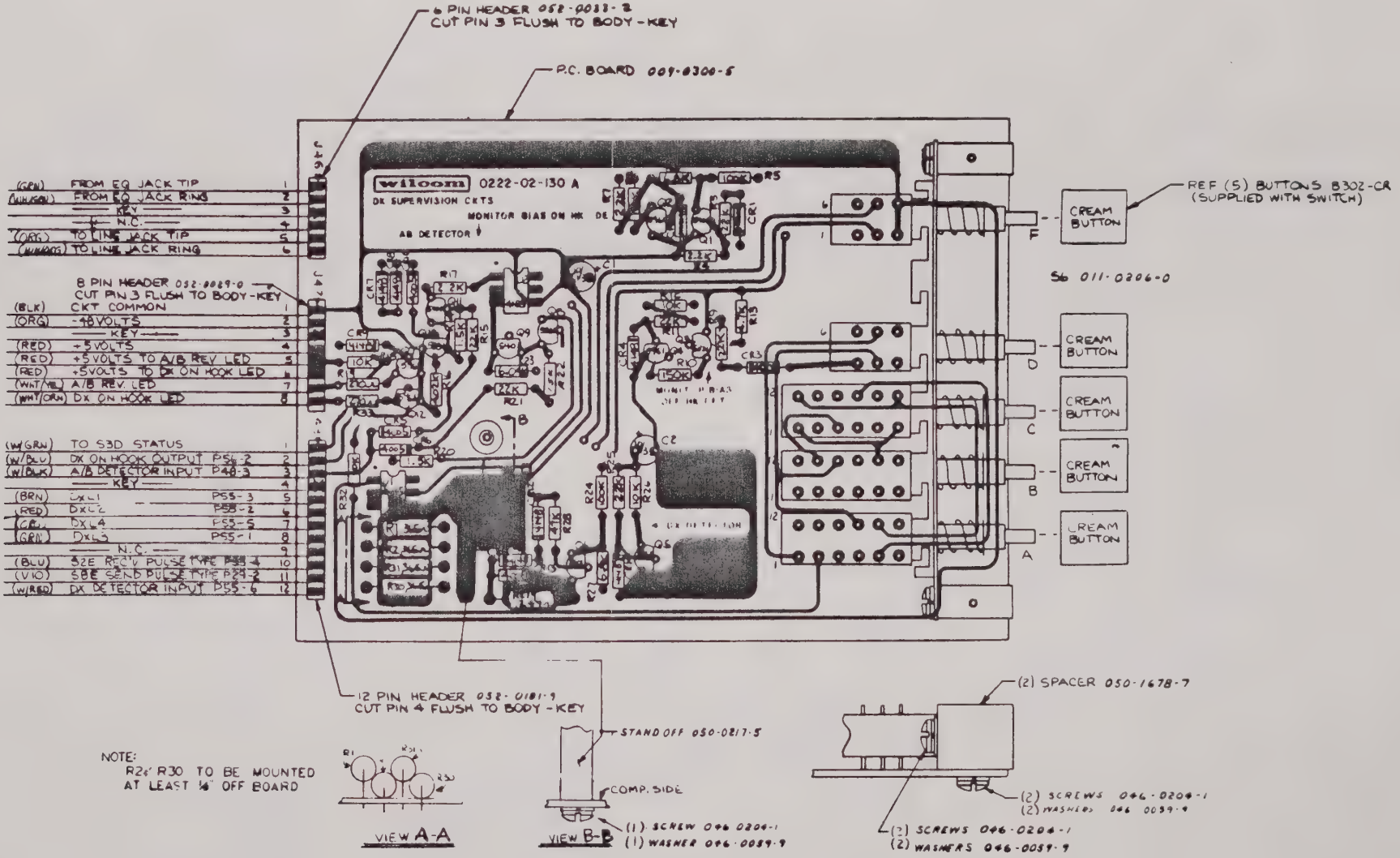


FIGURE 8-19
DX Supervision
PC Assembly A14

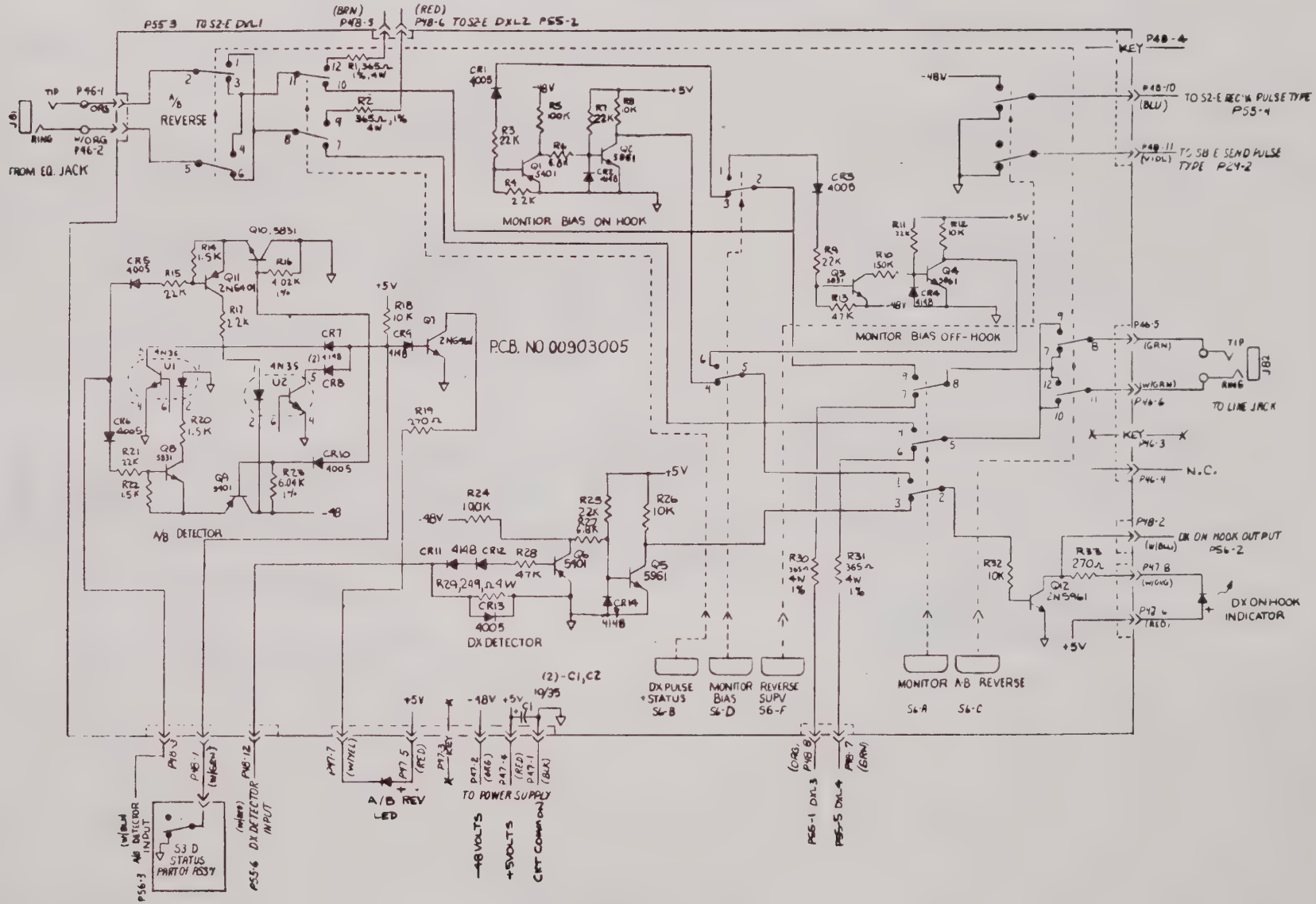


FIGURE 8-20
DX Supervision
Schematic A14

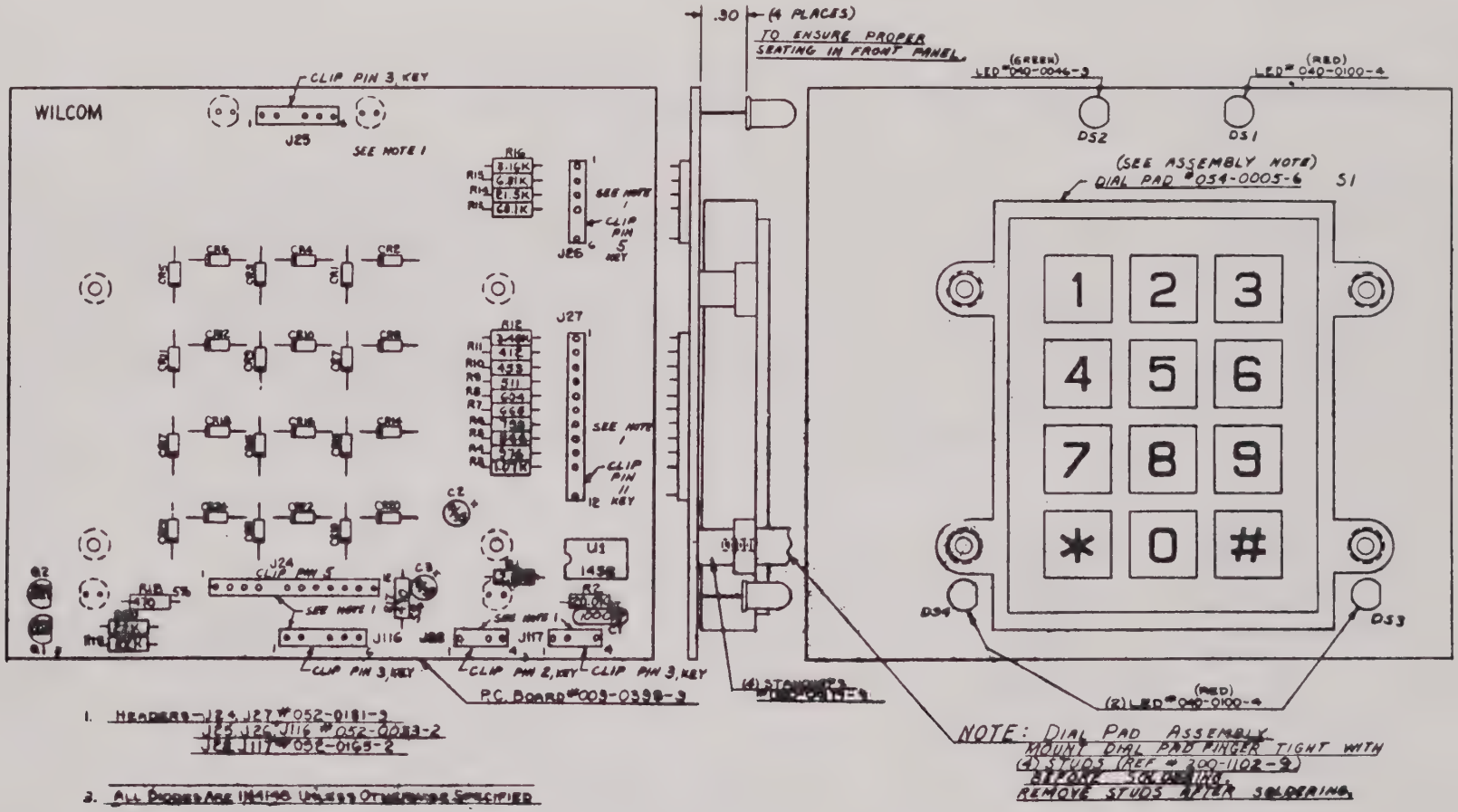


FIGURE 8-21
Keyboard and SF Attenuator
PC Assembly A15

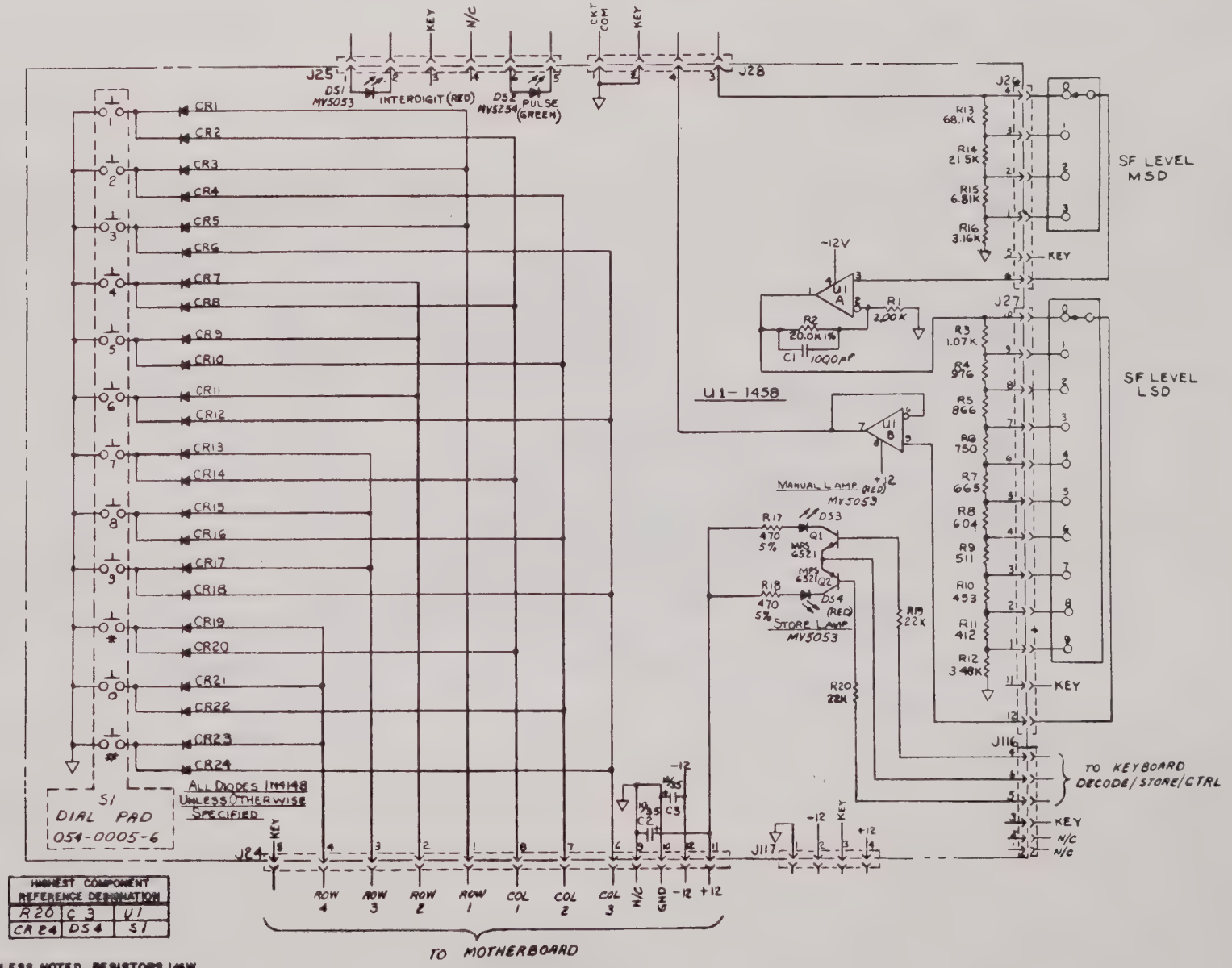
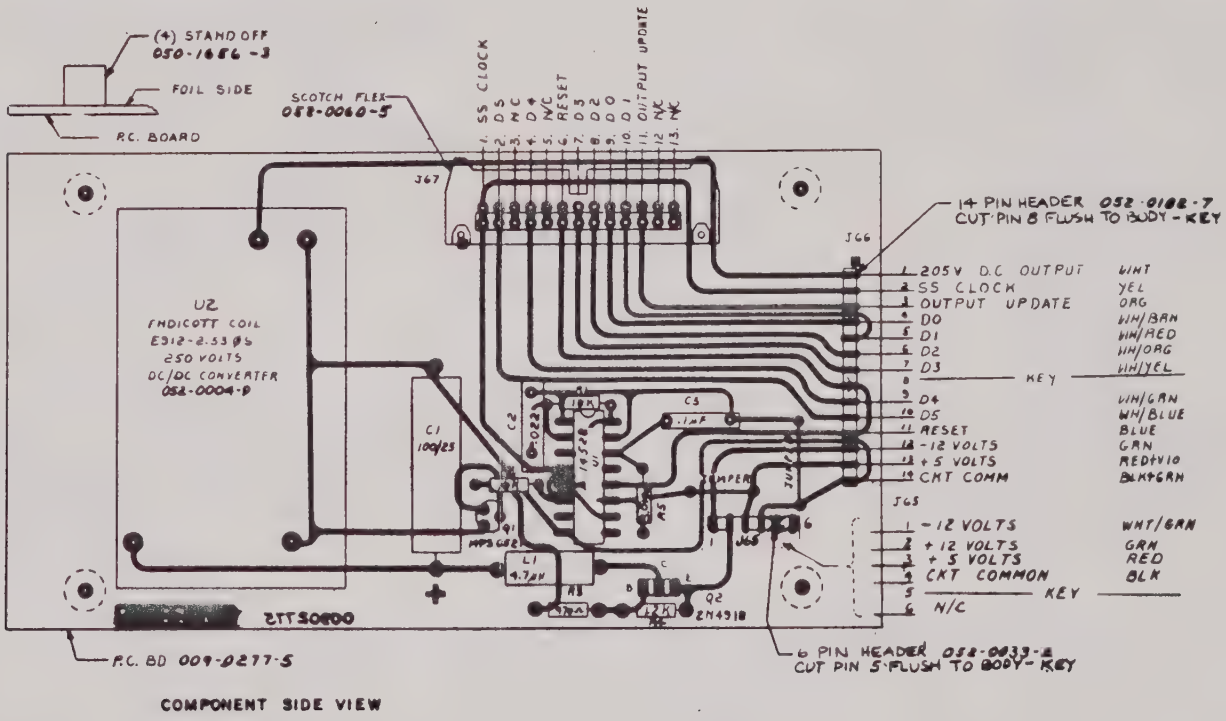


FIGURE 8-22
Keyboard and SF Attenuator
Schematic A15



COMPONENT SIDE VIEW

FIGURE 8-23
12 to 250 volt Converter
PC Assembly A16

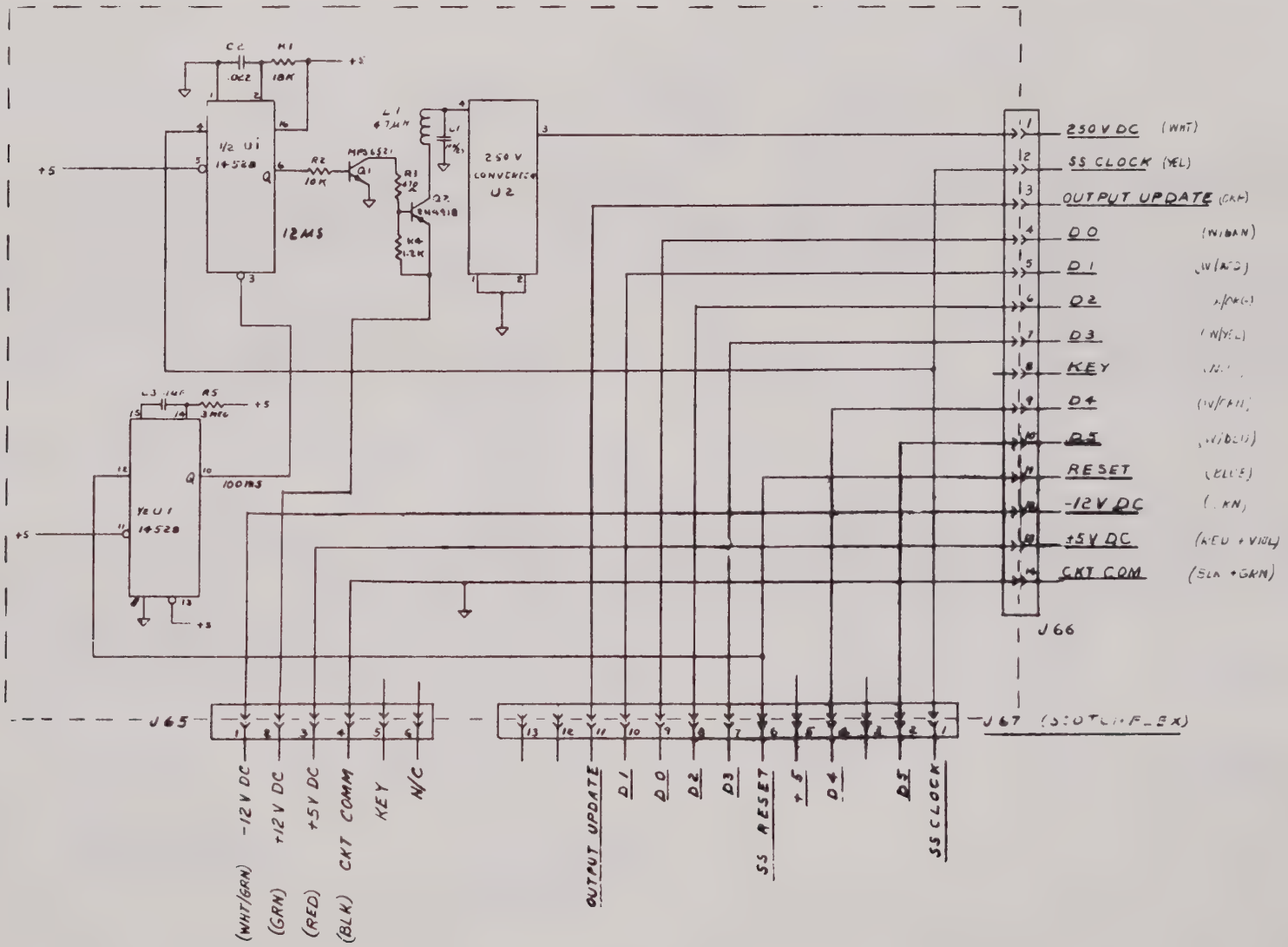
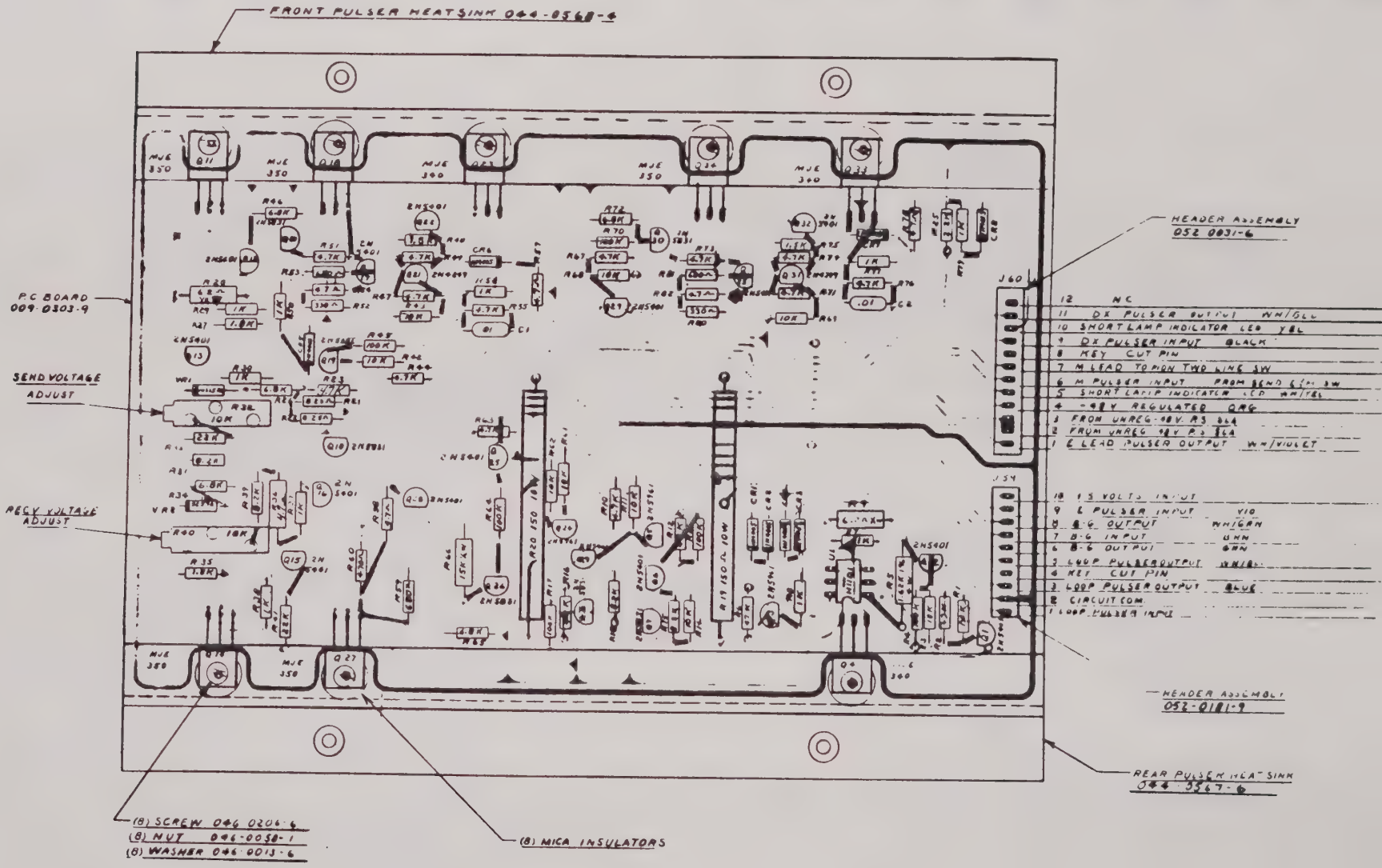


FIGURE 8-24
12-250 V Converter
Schematic A16



UNLESS NOTED, RESISTORS 1/4W
3 PLACE VALUES ±1% OTHERS ±5%

FIGURE 8-25
Loop and Line Pulser
PC Assembly A17

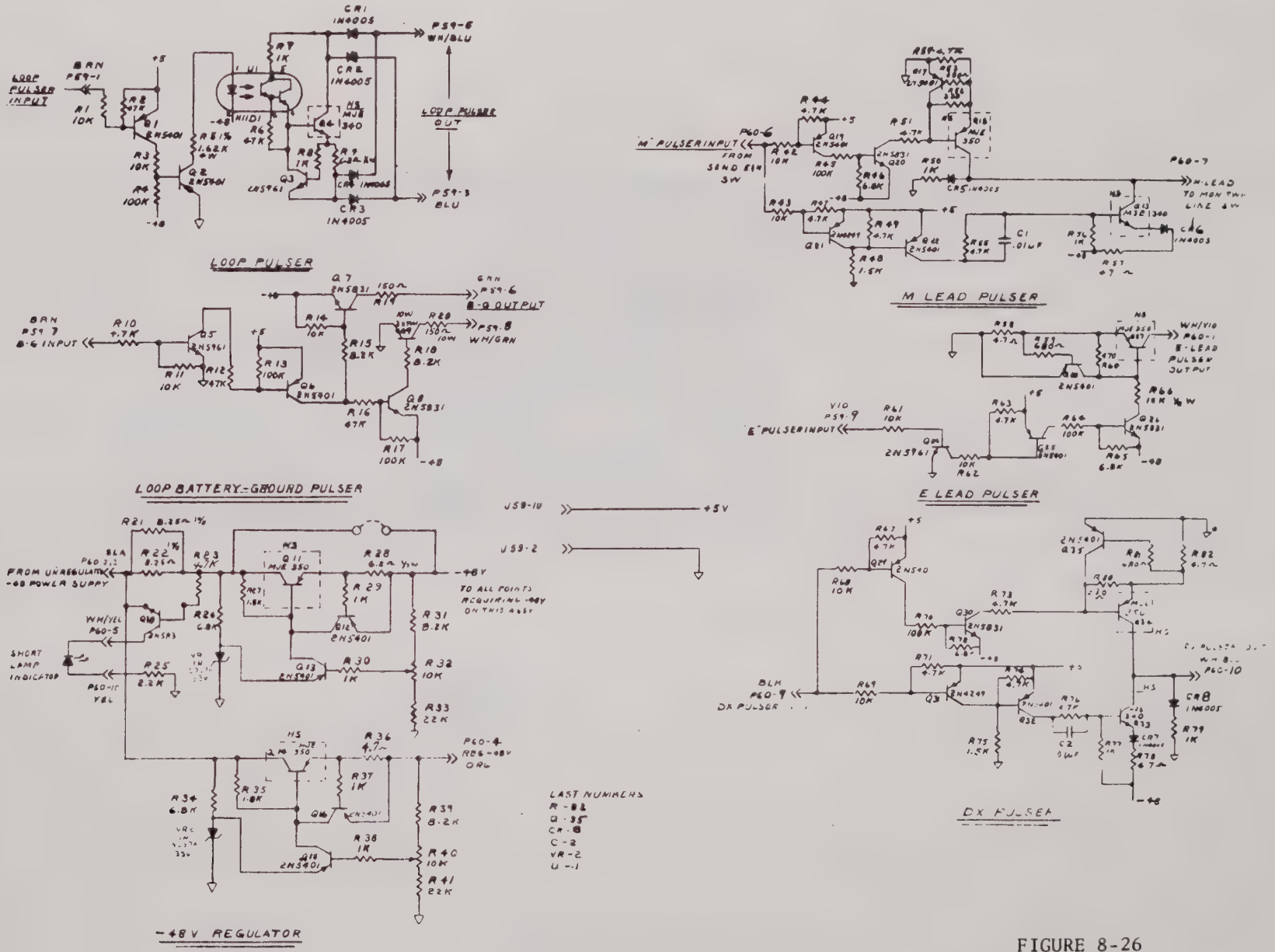


FIGURE 8-26
Loop & Line Pulser

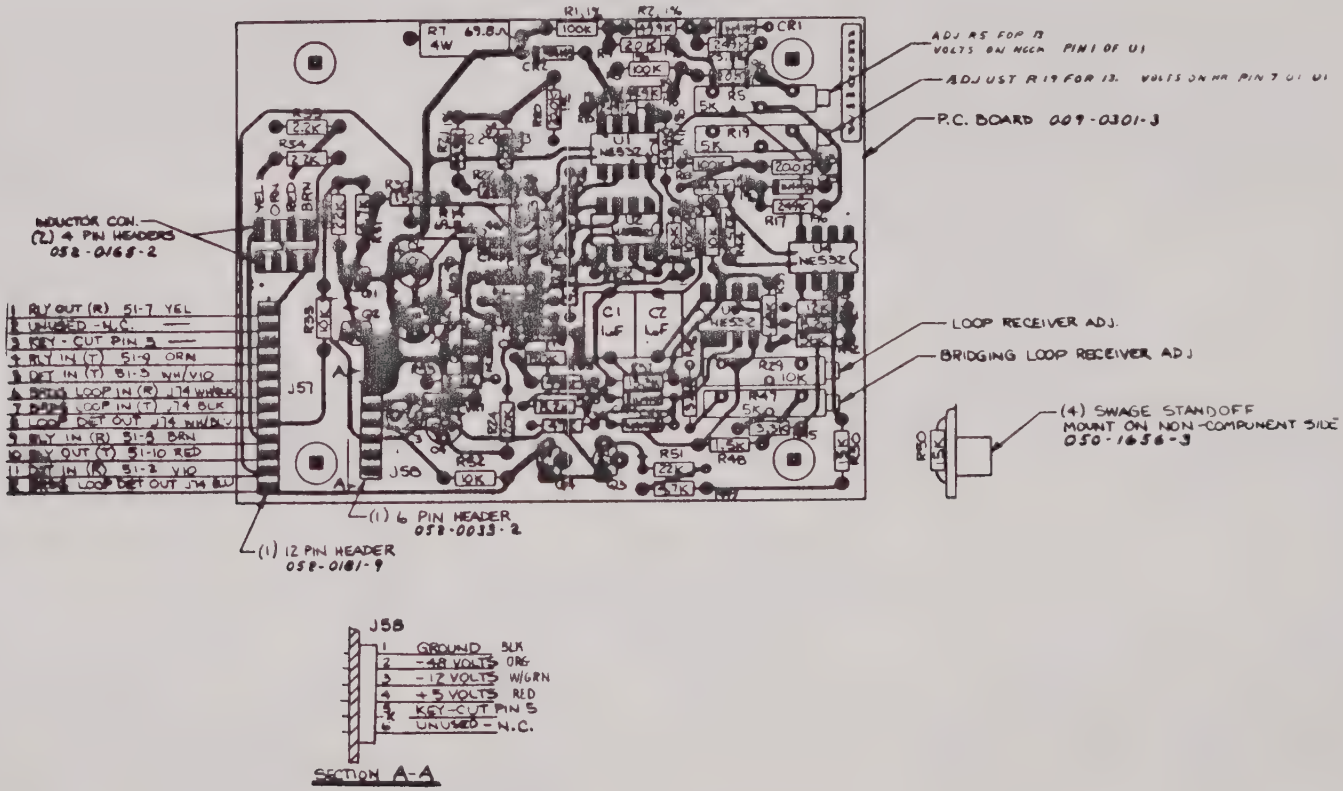


FIGURE 8-27
Loop Detector
PC Assembly A18

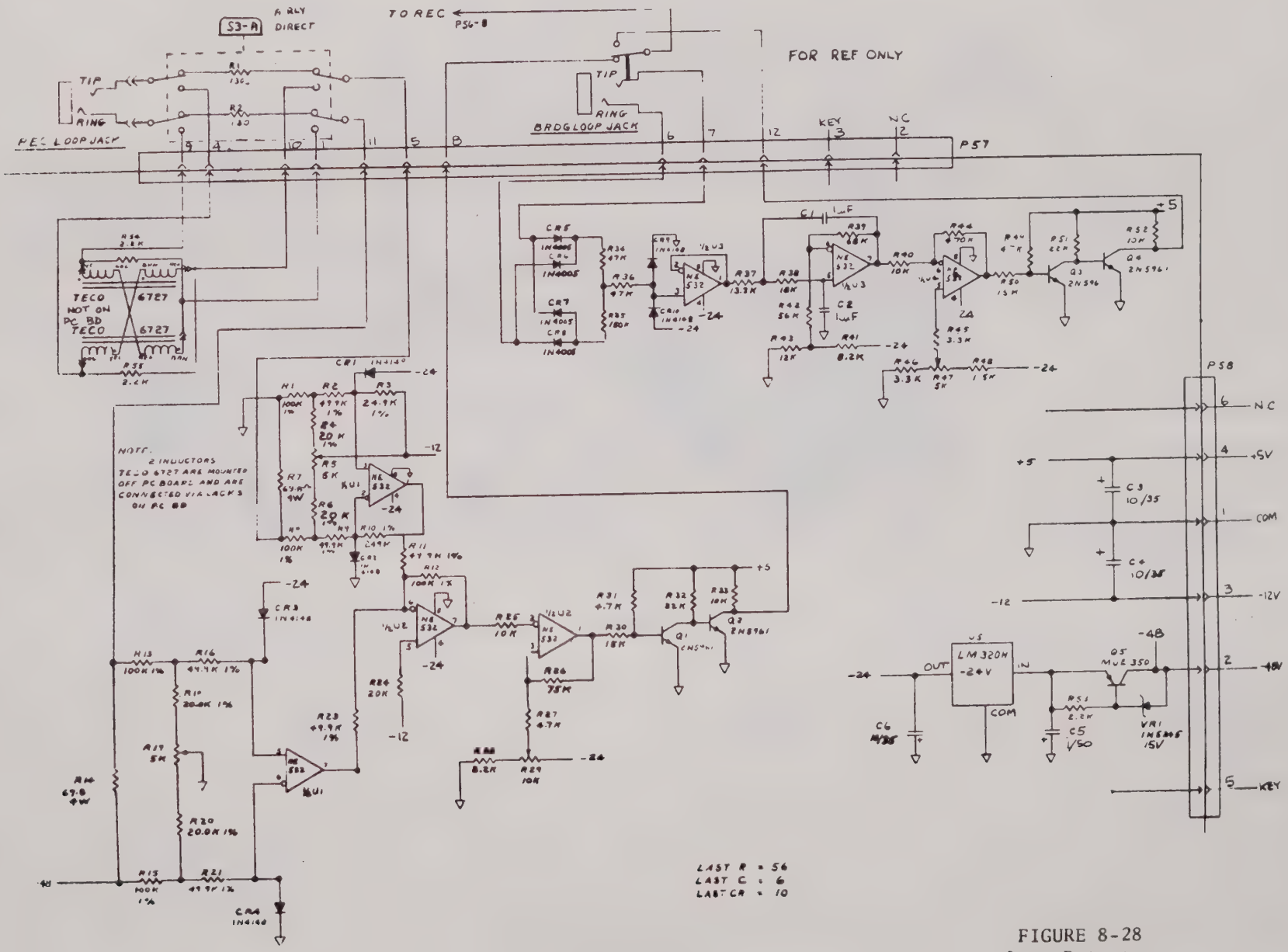


FIGURE 8-28
Loop Detector

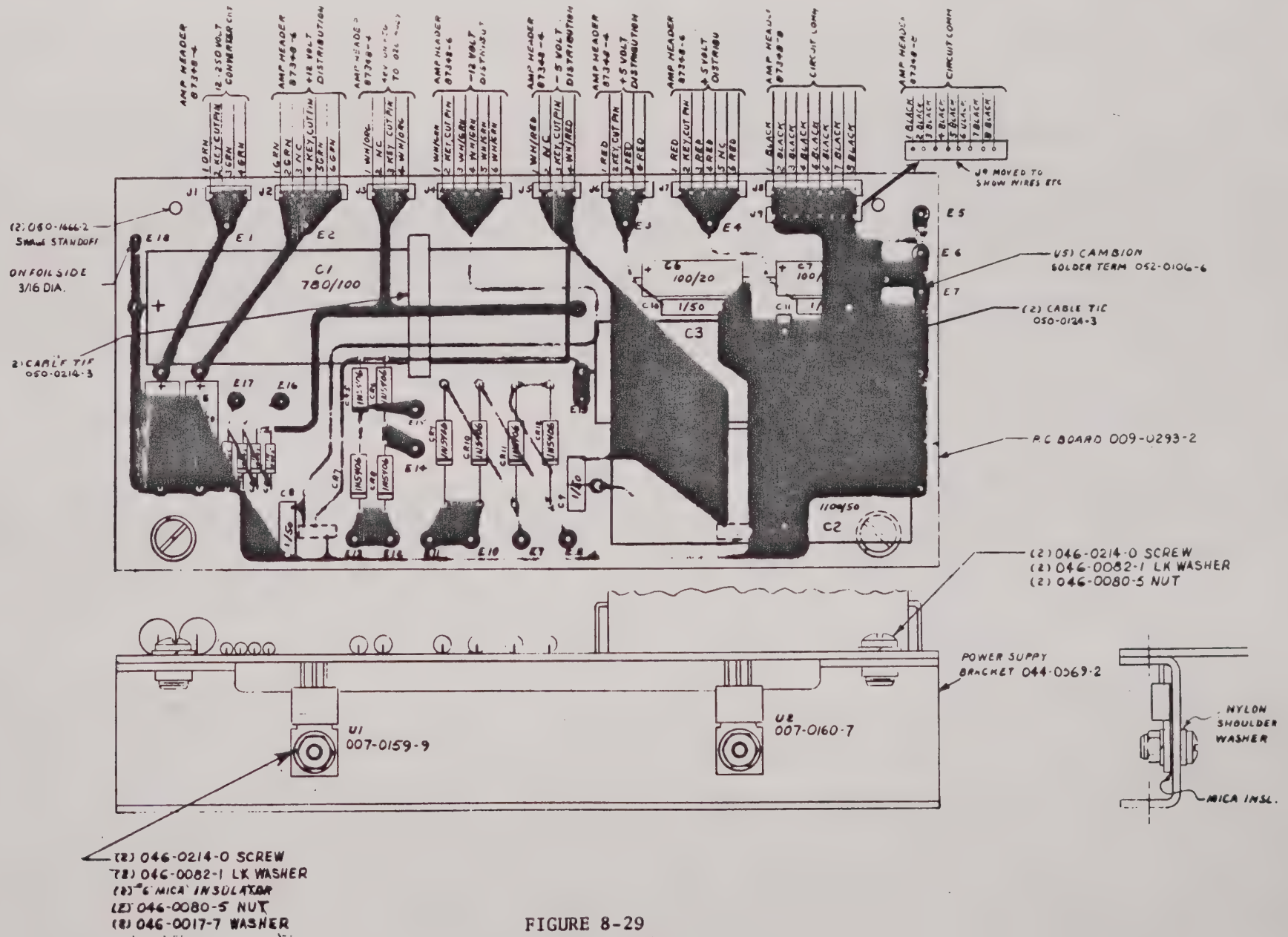


FIGURE 8-29
Power Supply 115V/230V
PC Assembly A19

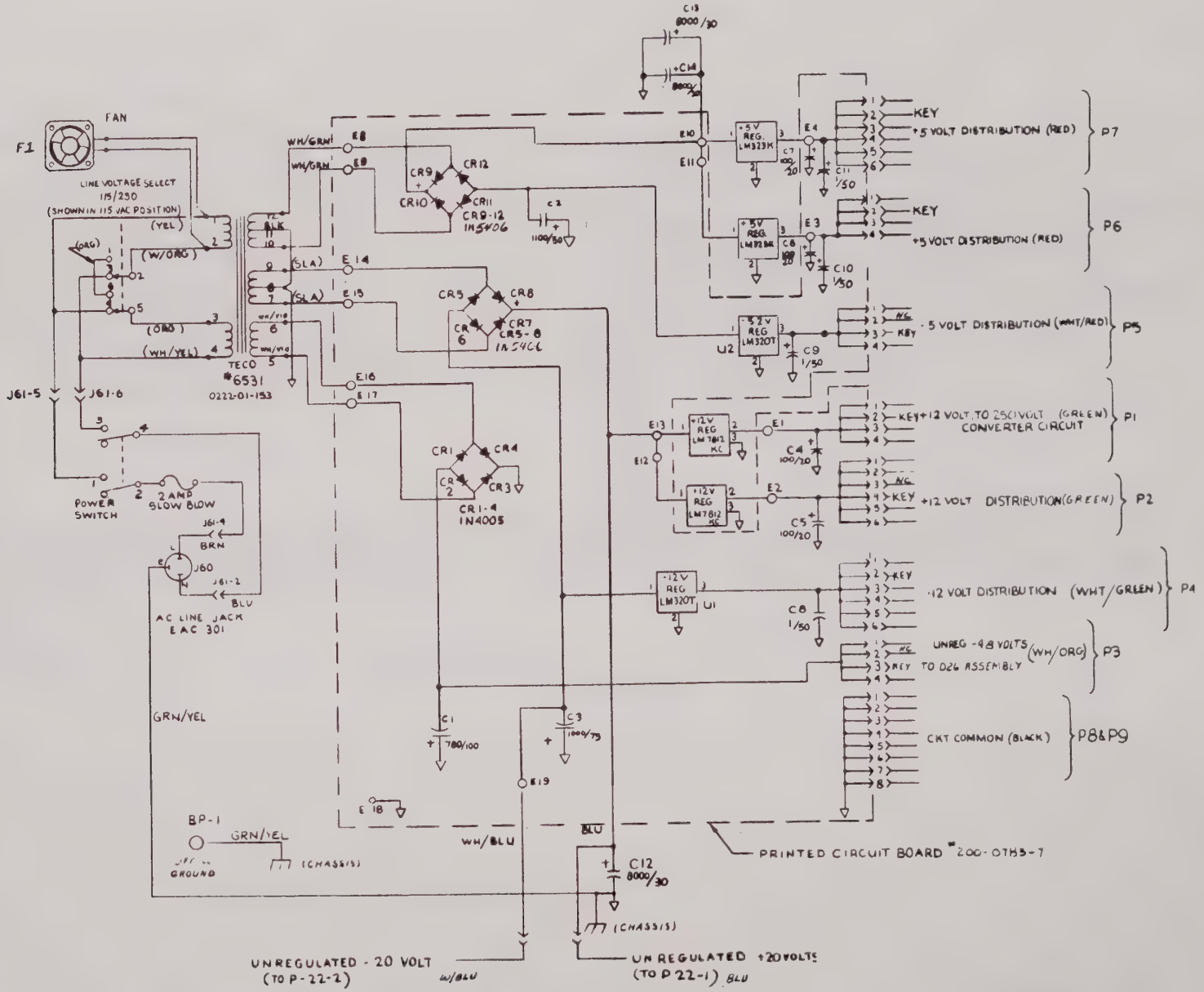


FIGURE 8-30
115/230 AC Option
Power Supply Schematic A19

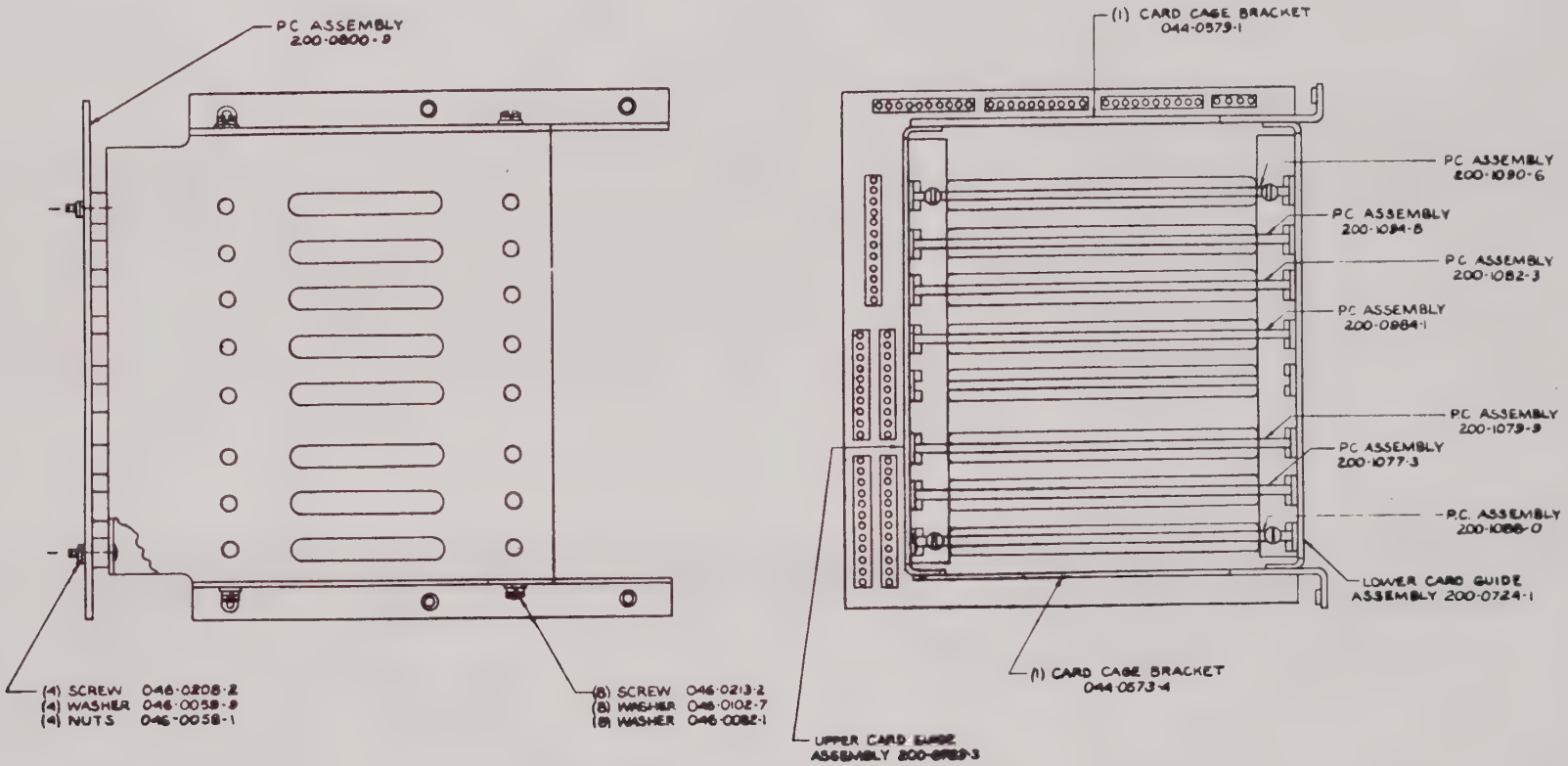


FIGURE 8-31
Card Cage Assembly A20

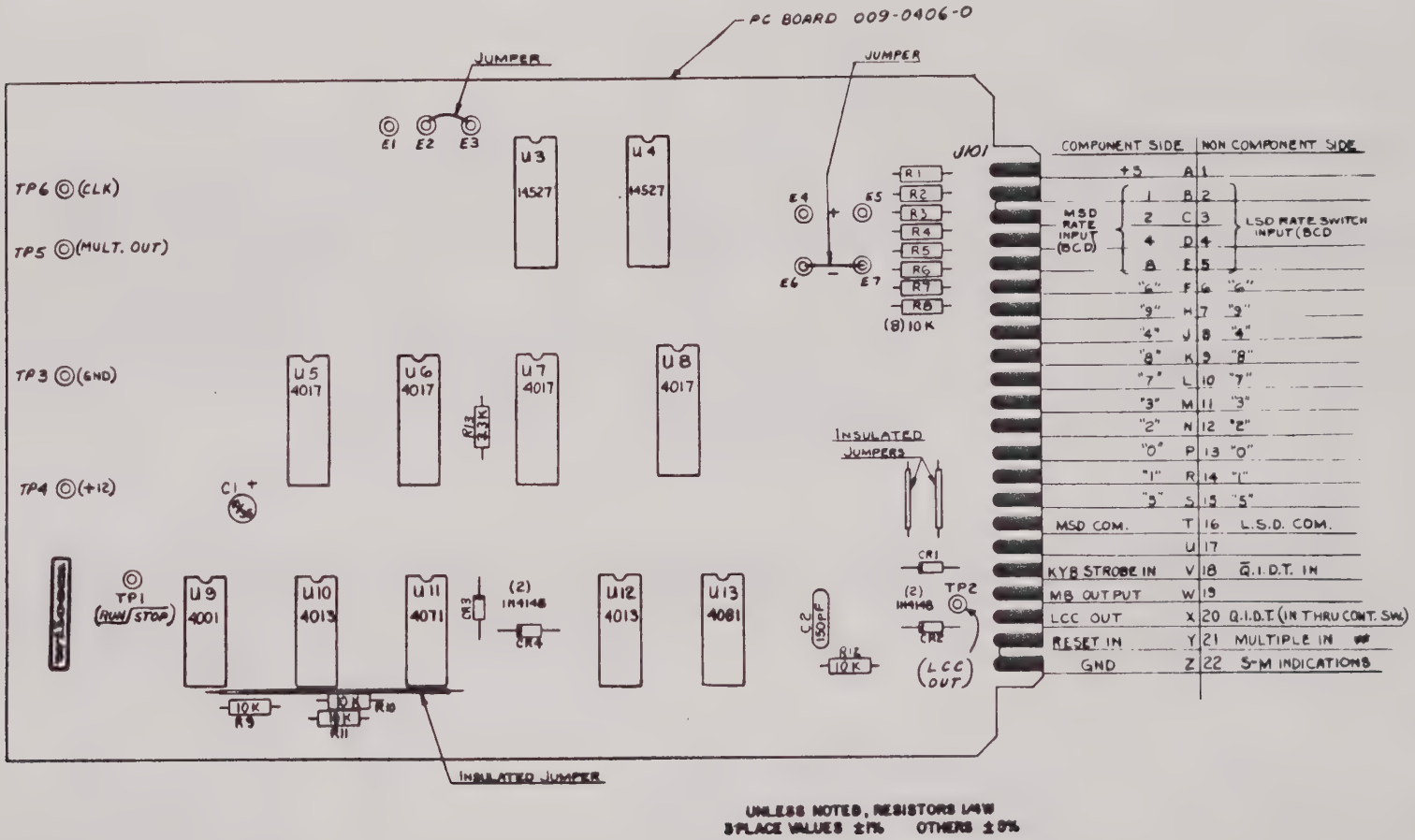
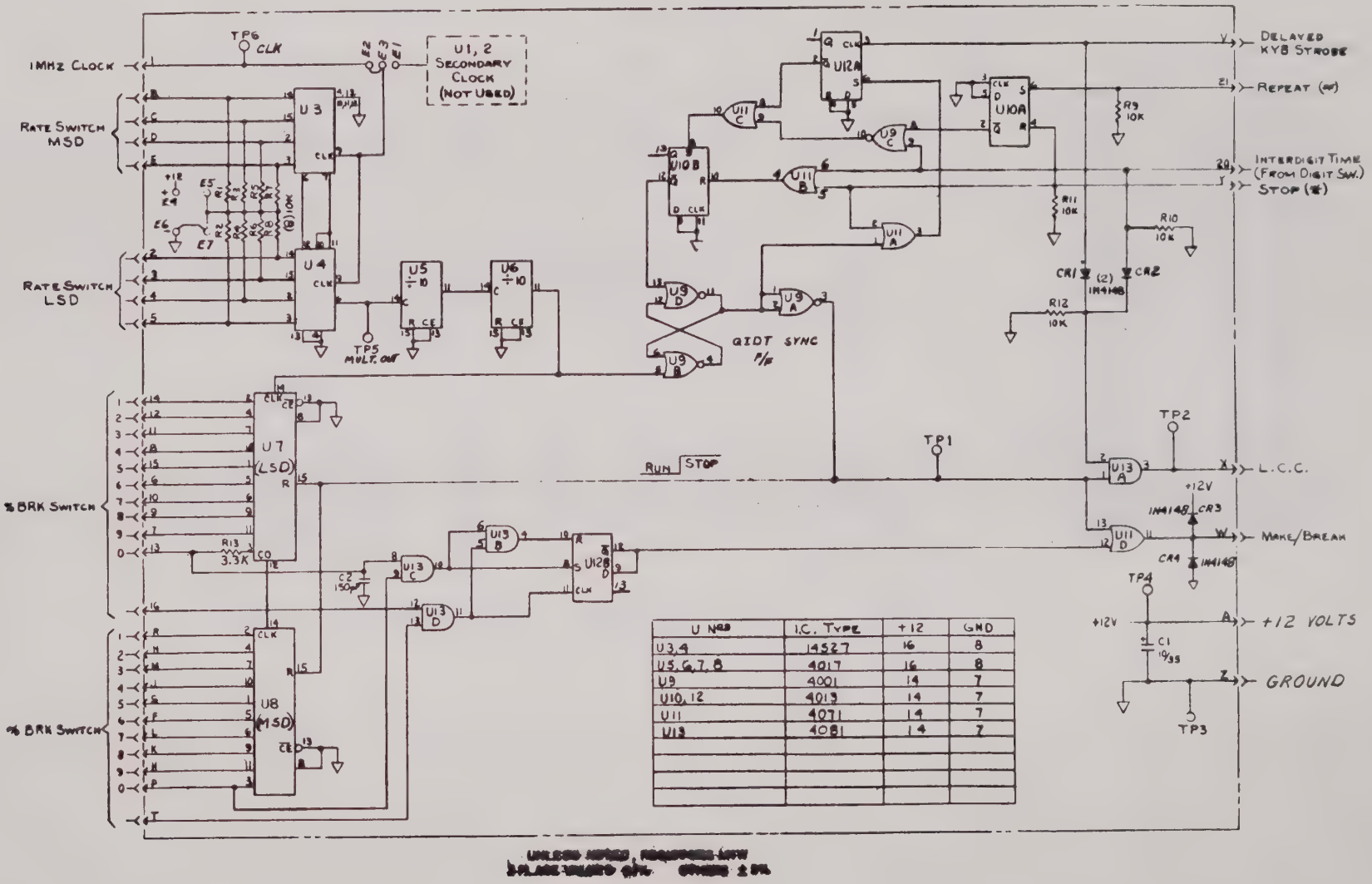


FIGURE 8-32
Rate % Break Generator
PC Assembly A21



U No.	I.C. Type	+12	GND
U3,4	14527	16	8
U5,6,7,8	4017	16	8
U9	4001	14	7
U10, 12	4013	14	7
U11	4071	14	7
U13	4081	14	7

FIGURE 8-33
Rate % Break Generator
Schematic 121

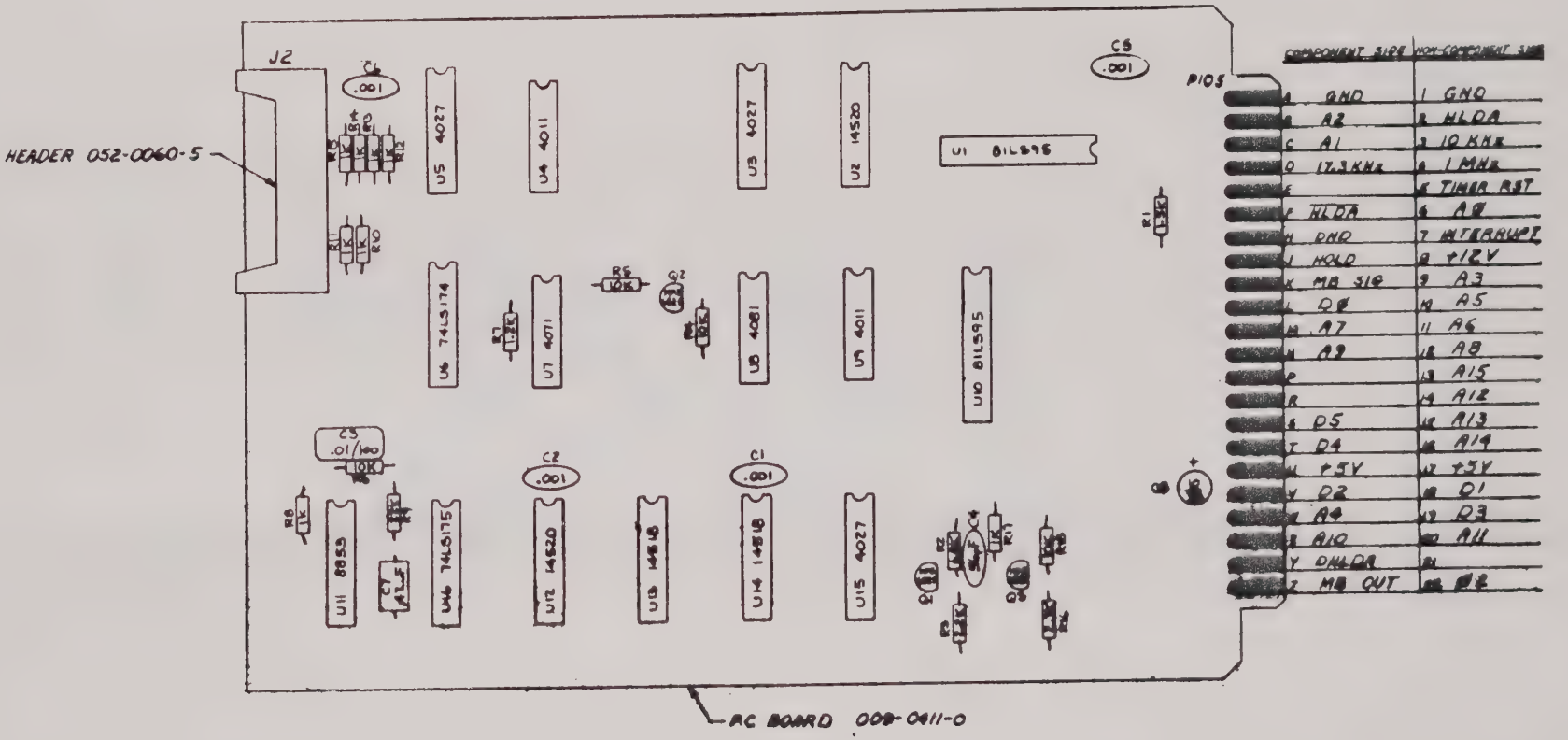
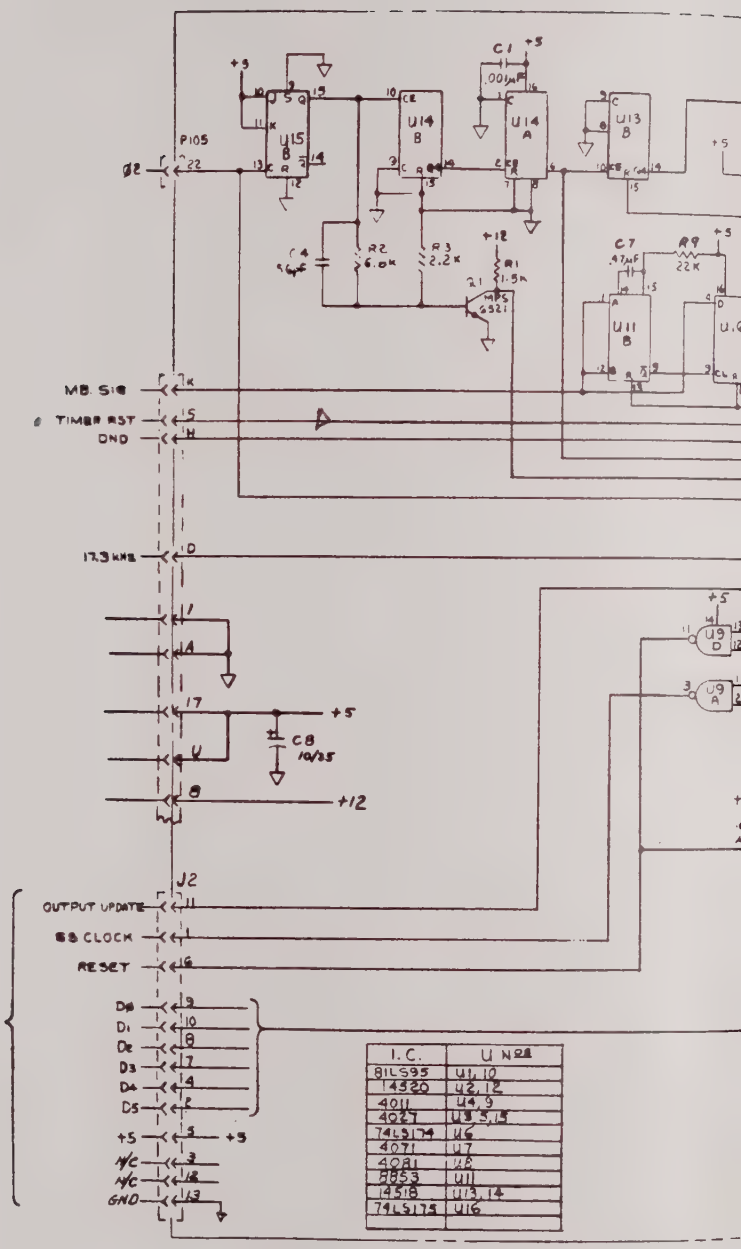
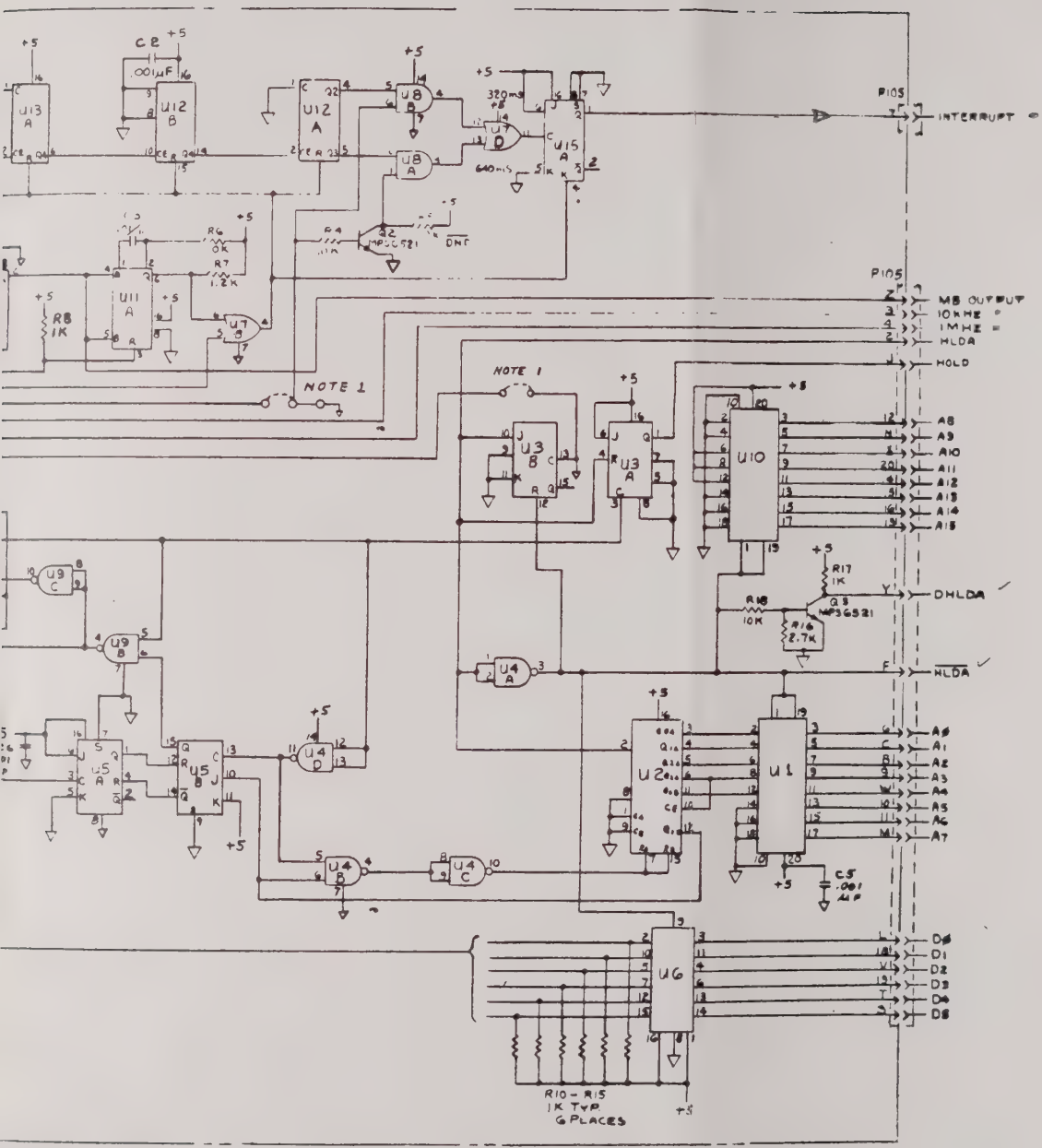


FIGURE 8-34
Interrupt Timer & Self-Scan Interface
PC Assembly A23



I.C.	U NOS
81LS95	U1, 10
14320	U2, 12
4011	U4, 9
4027	U3, 5, 15
74LS174	U6
4071	U7
4081	U8
8253	U11
14518	U13, 14
74LS175	U16



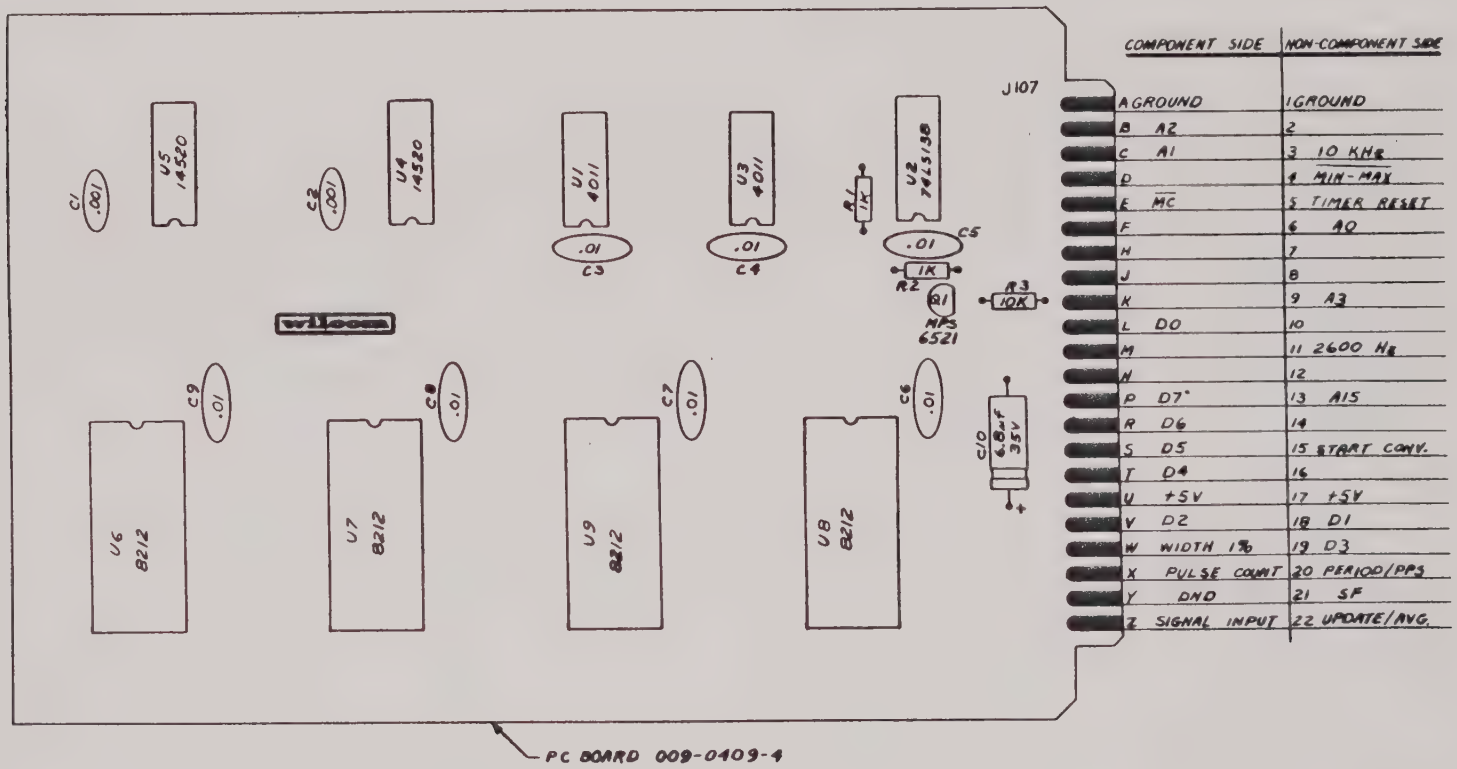
HIGHEST COMPONENT REFERENCE DESIGNATION		
A18	C8	Q3
U16		

UNUSED COMPONENT REFERENCE DESIGNATIONS		
U7A	U7C	U8C
U8D		

NOTE 1:
OPTIONS NOT USED ON PRODUCTION UNITS

2: UNLESS NOTED, RESISTORS 1/4W
3 PLACE VALUES ±1% OTHERS ±5%

FIGURE 8-35
Interrupt Timer and Self Scan Interface
Schematic A23



UNLESS NOTED, RESISTORS 1/4W
3 PLACE VALUES ±1% OTHERS ±5%

FIGURE 8-36
Data Input Control
PC Assembly A24

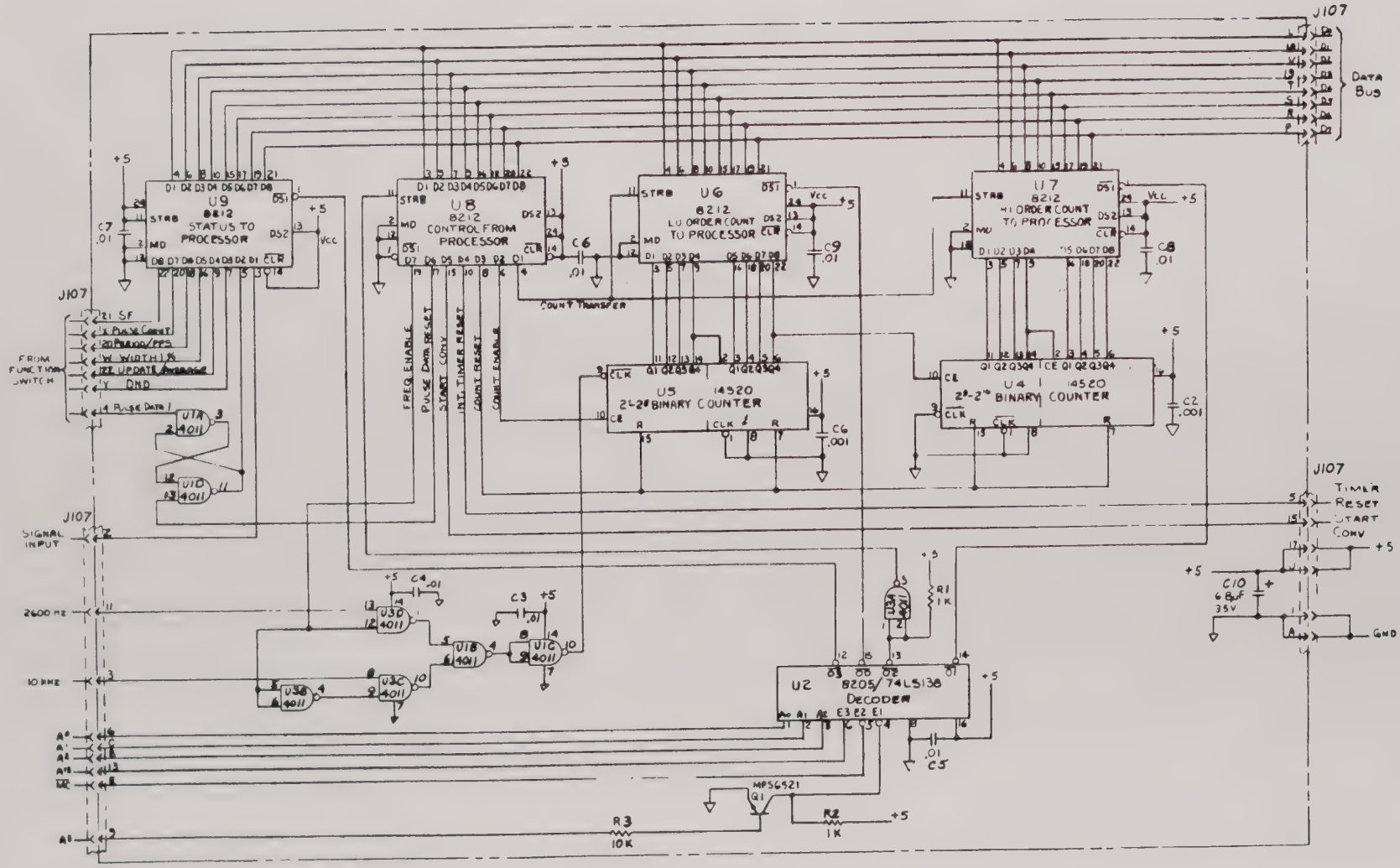
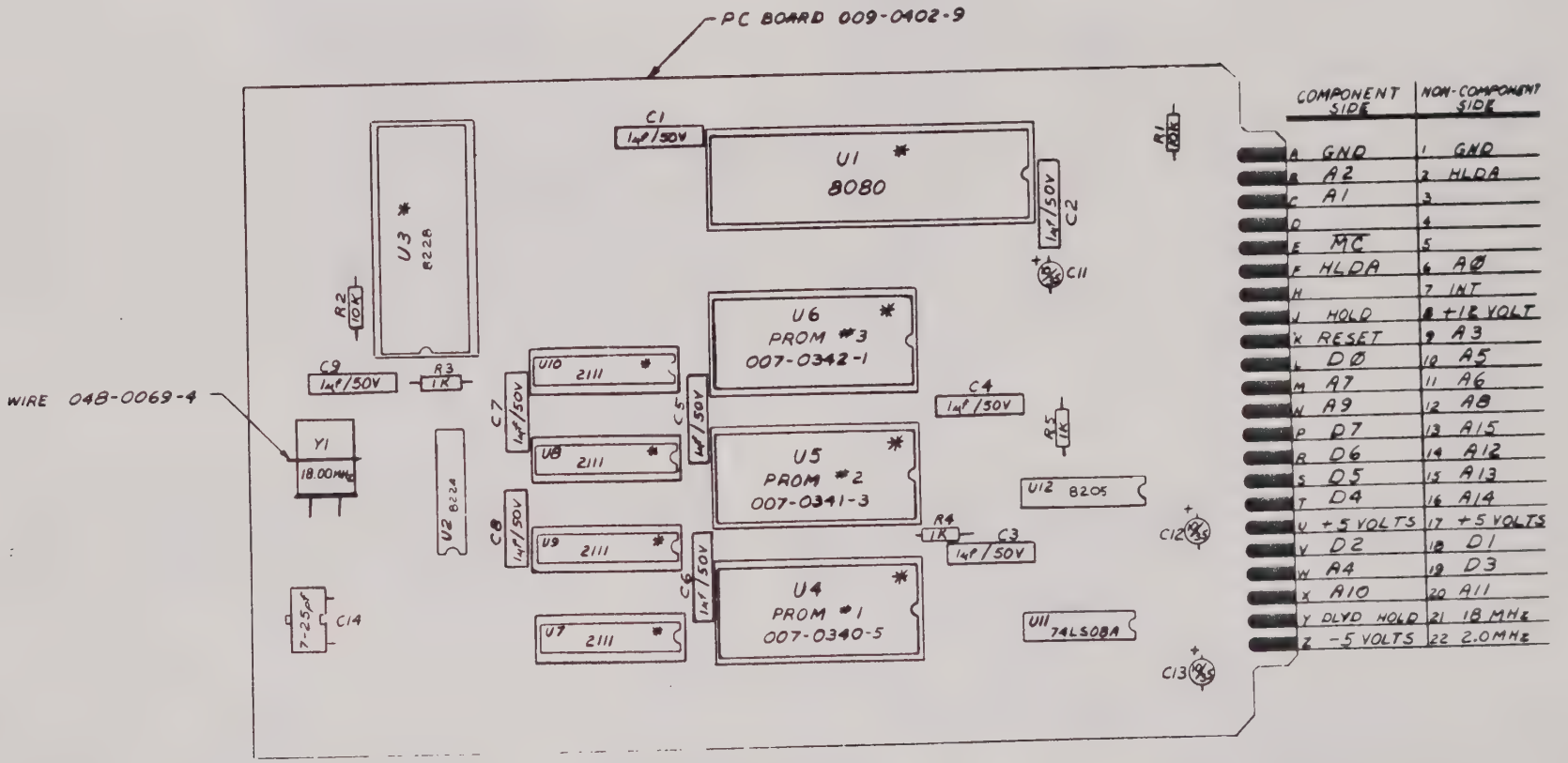
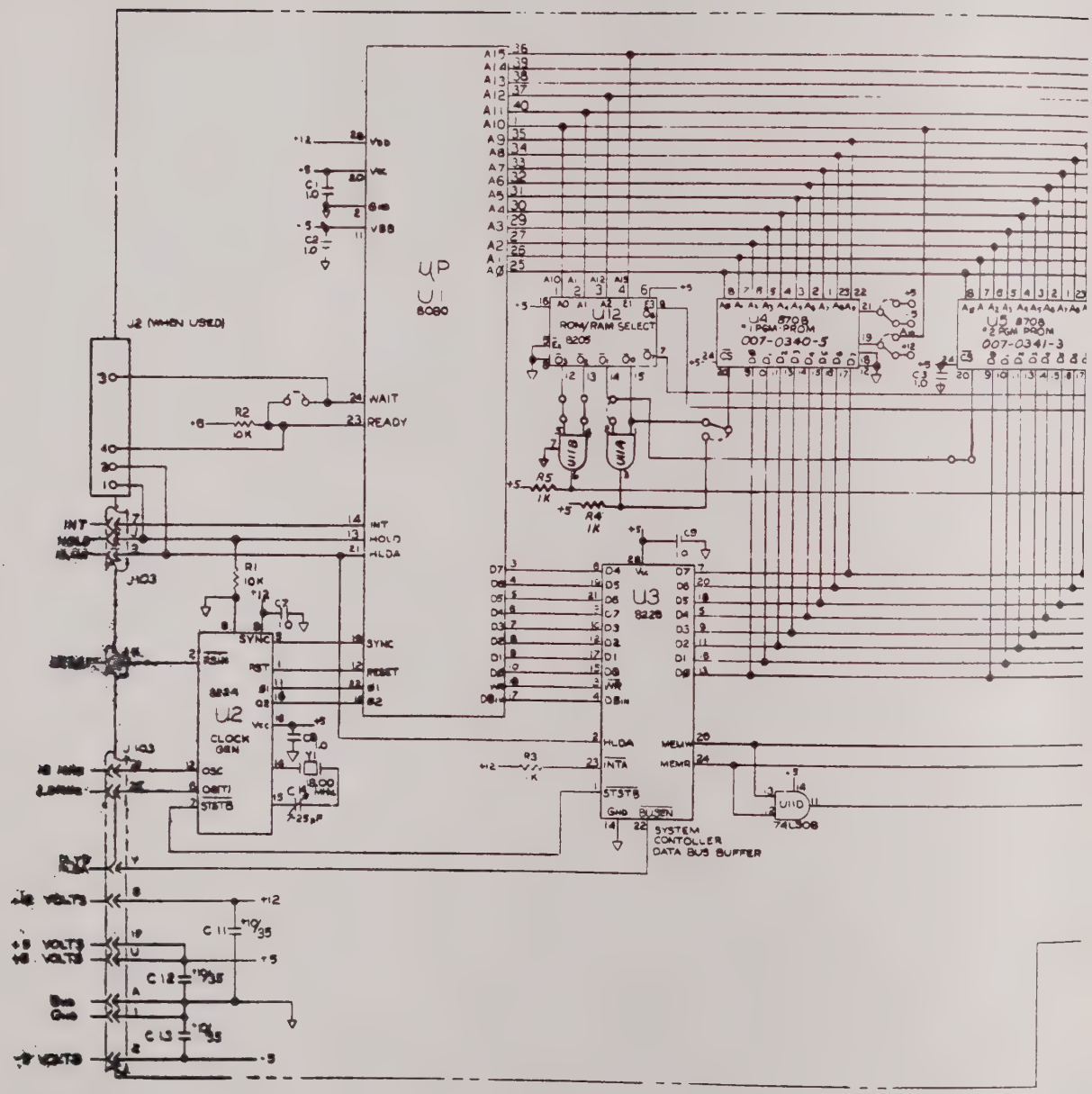


FIGURE 8-37
Data Input Control
Schemati—24



NOTES: * INSERTED IN SOCKETS
(1) 050-1636-5 FOR U1
(1) 050-1637-3 FOR U3
(3) 050-1640-7 FOR U4, 5, & 6
(4) 050-2004-5 FOR U7, 8, 9, & 10
UNLESS NOTED, RESISTORS 1/4W
3 PLACE VALUES ±1% OTHERS ±5%

FIGURE 8-38
CPU
PC Assembly A25



UP
U1
8080
U12
ROM/RAM SELECT
8205
U4 8708
1 PGM PROM
007-0340-5
U5 8708
2 PGM PROM
007-0341-3
U3
8228
U2
CLOCK GEN
8224
SYSTEM CONTOLLER DATA BUS BUFFER
74LS08
J2 (WHEN USED)
J103
WAIT
READY
INT
HOLD
HLDA
SYNC
RESET
OSC
STSTB
INTA
MEMW
MEMR
GND
BUSEN
+12 VOLTS
+5 VOLTS
+8 VOLTS
-5 VOLTS

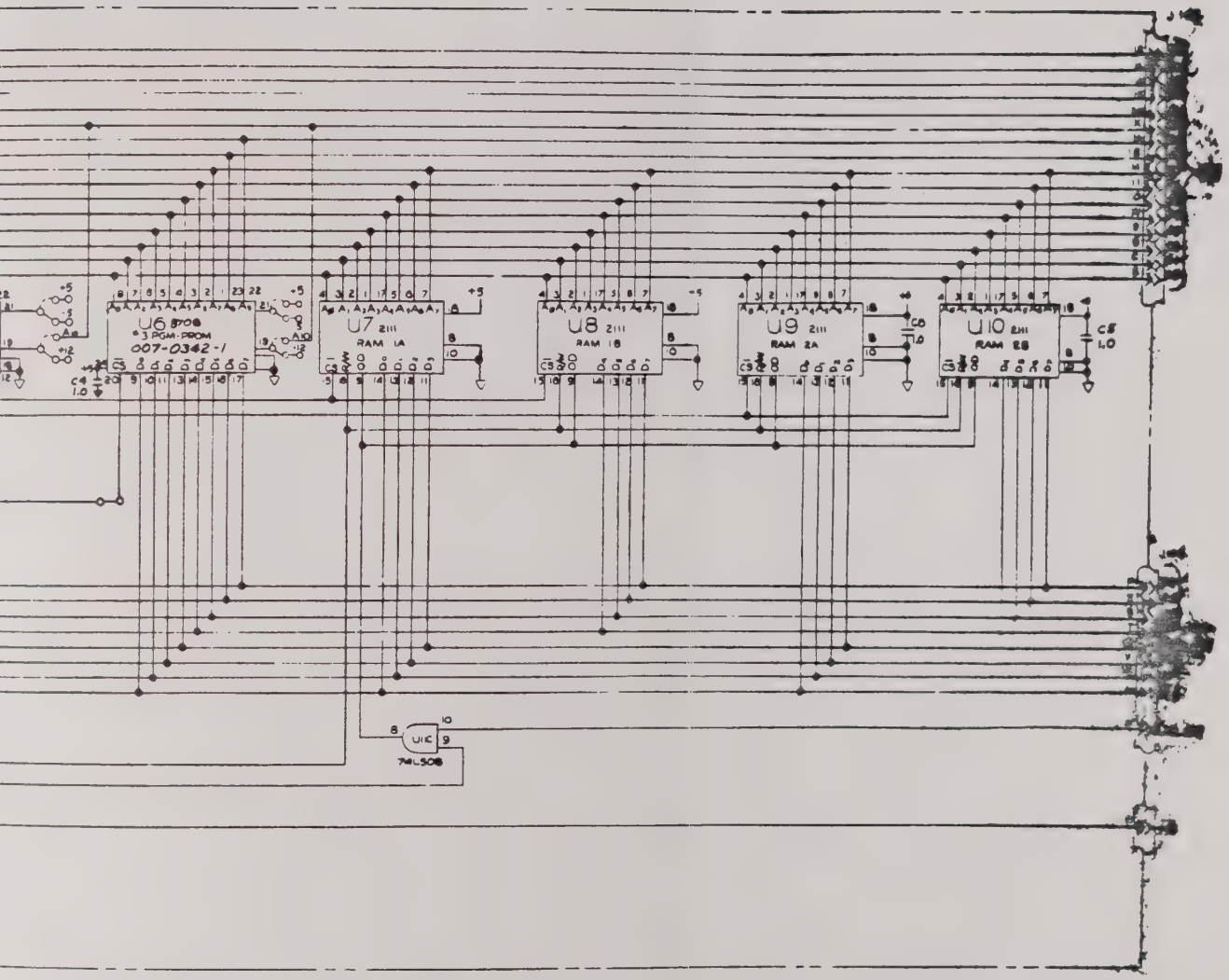
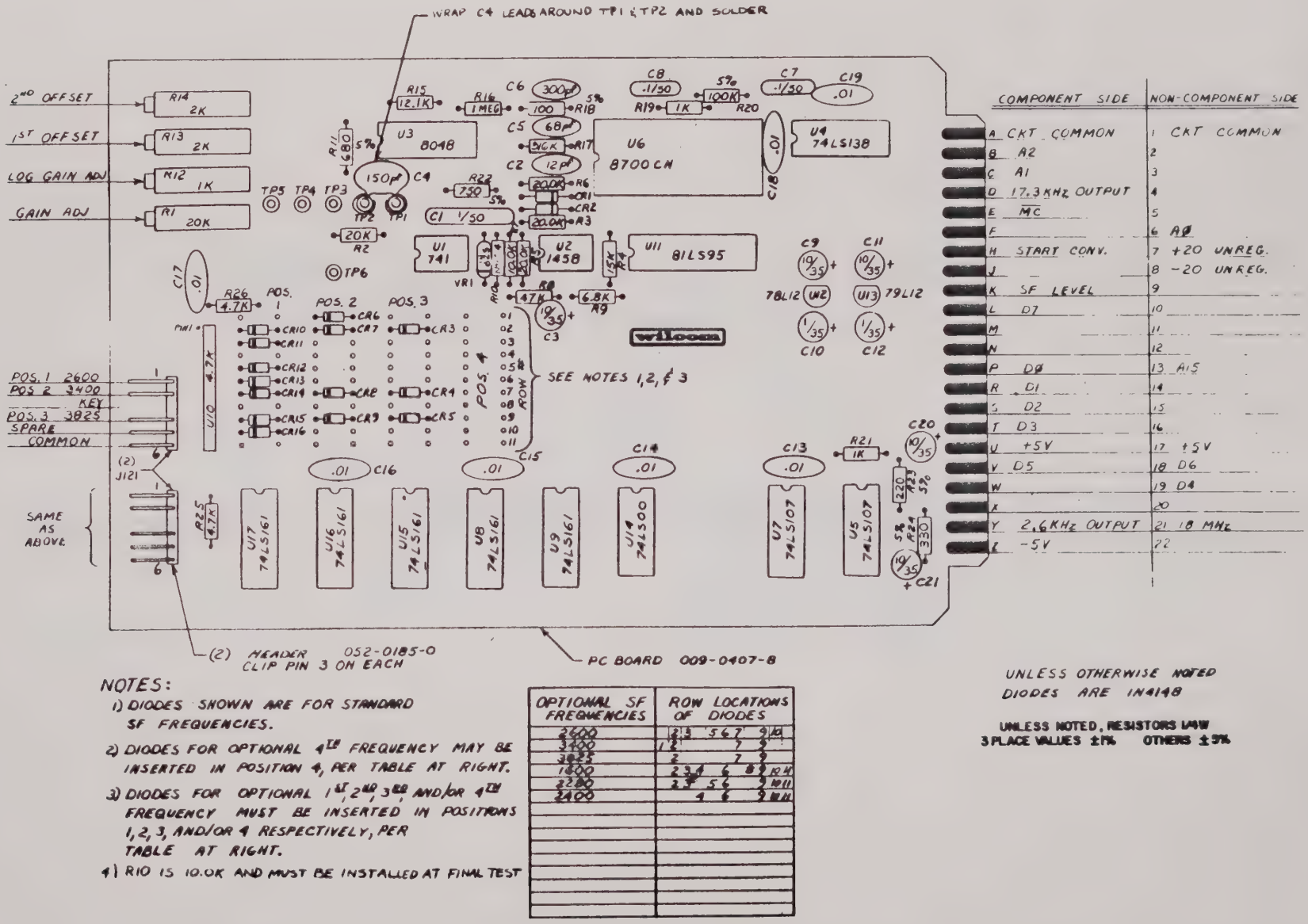


FIGURE 8-39
CPU
Schematic A25



NOTES:

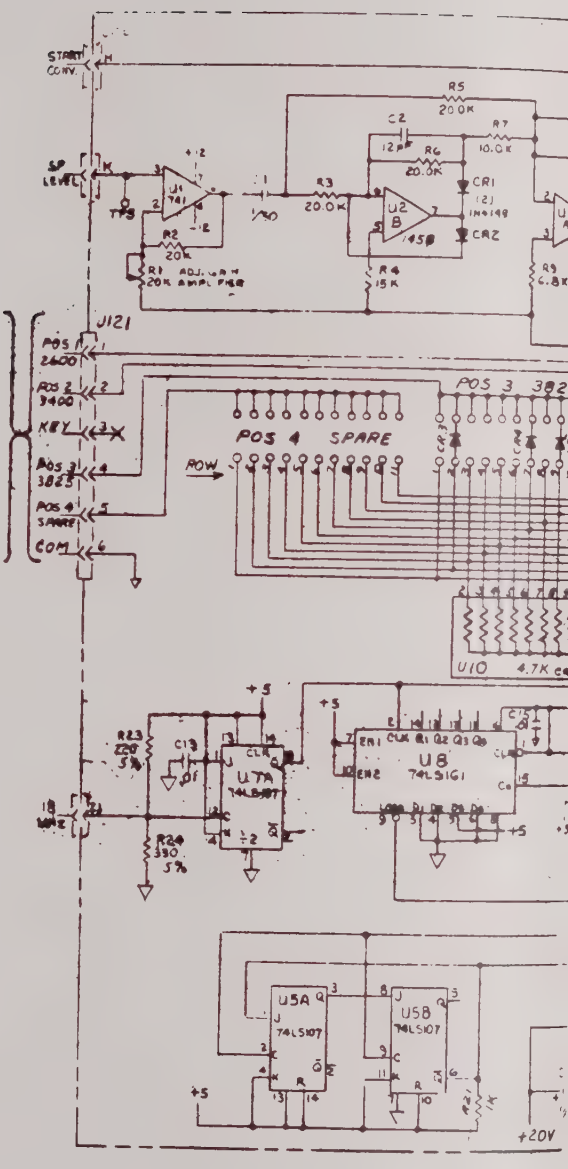
1) DIODES SHOWN ARE FOR STANDARD SF FREQUENCIES.
2) DIODES FOR OPTIONAL 4TH FREQUENCY MAY BE INSERTED IN POSITION 4, PER TABLE AT RIGHT.
3) DIODES FOR OPTIONAL 1ST, 2ND, 3RD AND/OR 4TH FREQUENCY MUST BE INSERTED IN POSITIONS 1, 2, 3, AND/OR 4 RESPECTIVELY, PER TABLE AT RIGHT.
4) R10 IS 10.0K AND MUST BE INSTALLED AT FINAL TEST

OPTIONAL SF FREQUENCIES	ROW LOCATIONS OF DIODES
2600	2 3 5 6 7 9 10
3400	1 2 7 9
3825	2 7 9
1800	2 3 4 6 8 9 10 H
2200	2 3 5 6 9 10 11
2400	4 6 9 10 11

UNLESS OTHERWISE NOTED DIODES ARE IN4148

UNLESS NOTED, RESISTORS 1/4W 3 PLACE VALUES ±1% OTHERS ±5%

FIGURE 8-40
A/D Converter & Frequency Divider
PC Assembly A26



NOTES:

1) DIODES SHOWN ARE FOR STANDARD SF FREQUENCIES
2) DIODES FOR OPTIONAL 4TH FREQ. MAY BE INSERTED IN POSITION 4, PER TABLE BELOW.
3) DIODES FOR OPTIONAL 1ST, 2ND, 3RD AND/OR 4TH FREQUENCY MUST BE INSERTED IN POSITIONS 1, 2, 3, AND/OR 4 RESPECTIVELY, PER TABLE BELOW.

OPTIONAL SF FREQUENCIES	ROW LOCATION OF DIODES
2600	2 3 6 7 9 10
3400	1 2 7 9
3825	6 7 9
1600	2 3 4 6 8 9 10 11
2280	3 5 9 10 11
2400	4 5 9 10 11

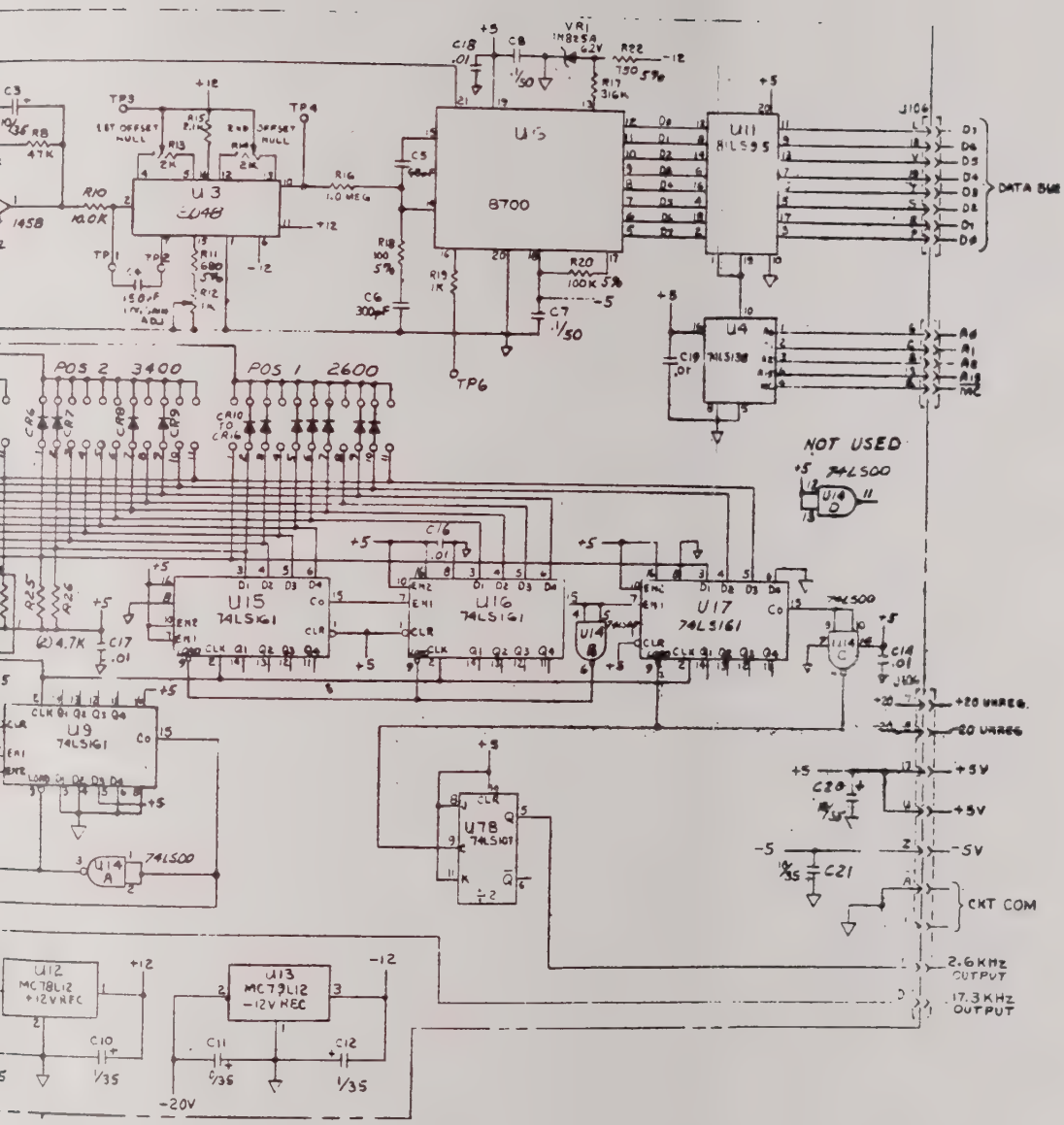


FIGURE 8-41
A/D Converter & Frequency Divider
Schematic A26

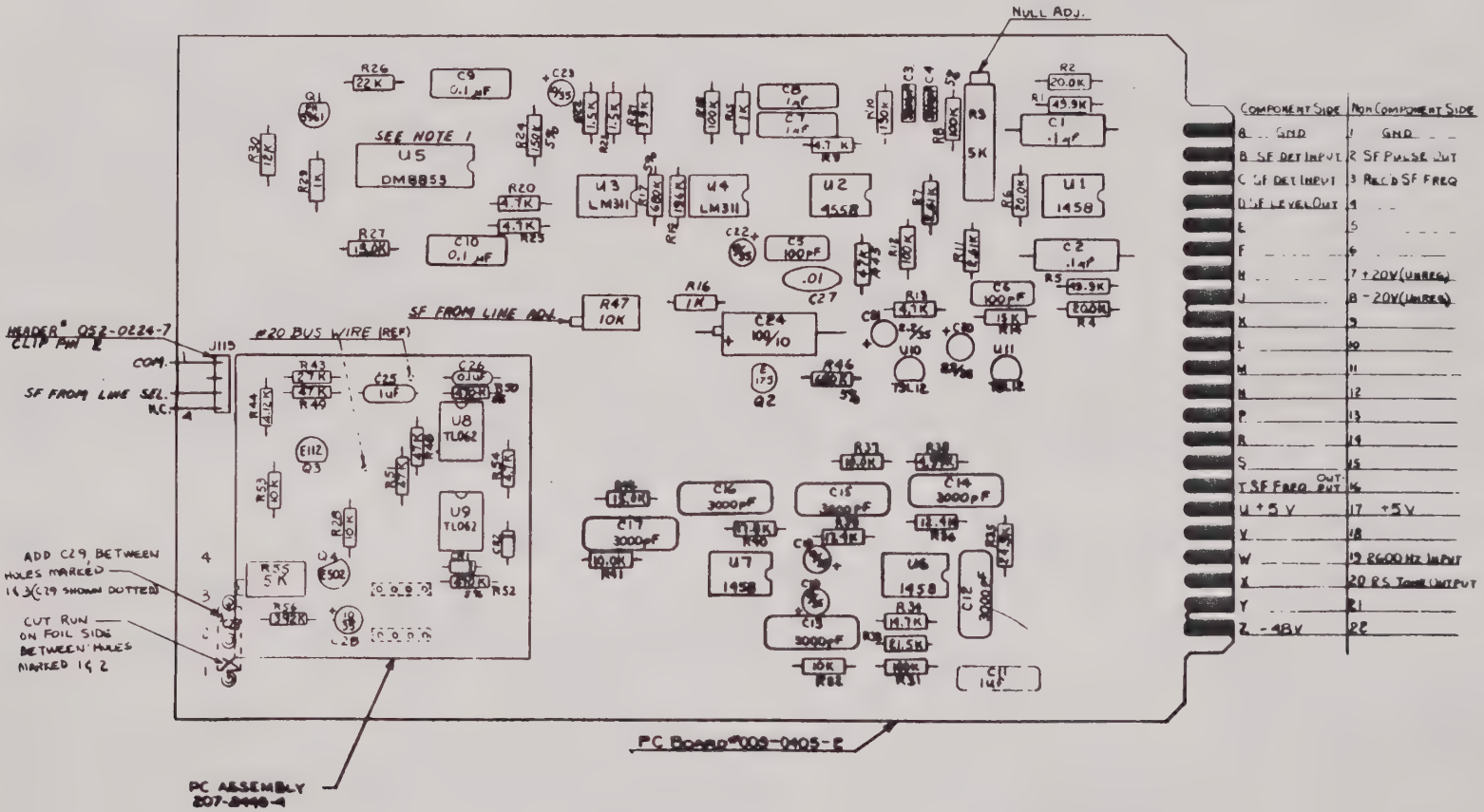
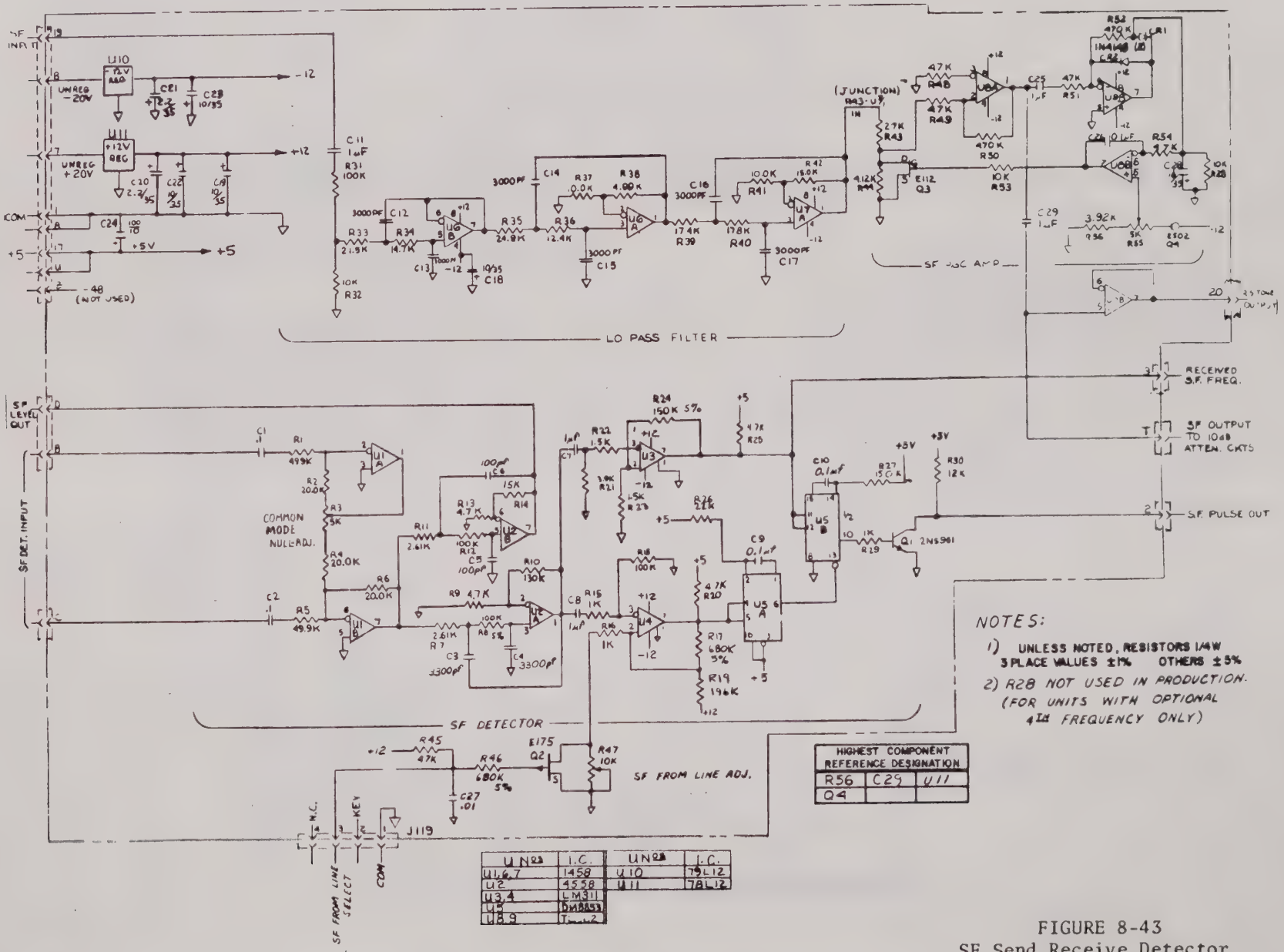


FIGURE 8-42
SF Send Receive Detector
PC Assembly A27



HIGHEST COMPONENT REFERENCE DESIGNATION		
R56	C29	U11
Q4		

U Nos	I.C.	U Nos	I.C.
U1,6,7	1458	U10	79L12
U2	4558	U11	78L12
U3,4	LM311		
U5	DM8833		
U8,9	TL072		

FIGURE 8-43
SF Send Receive Detector
Schematic A27

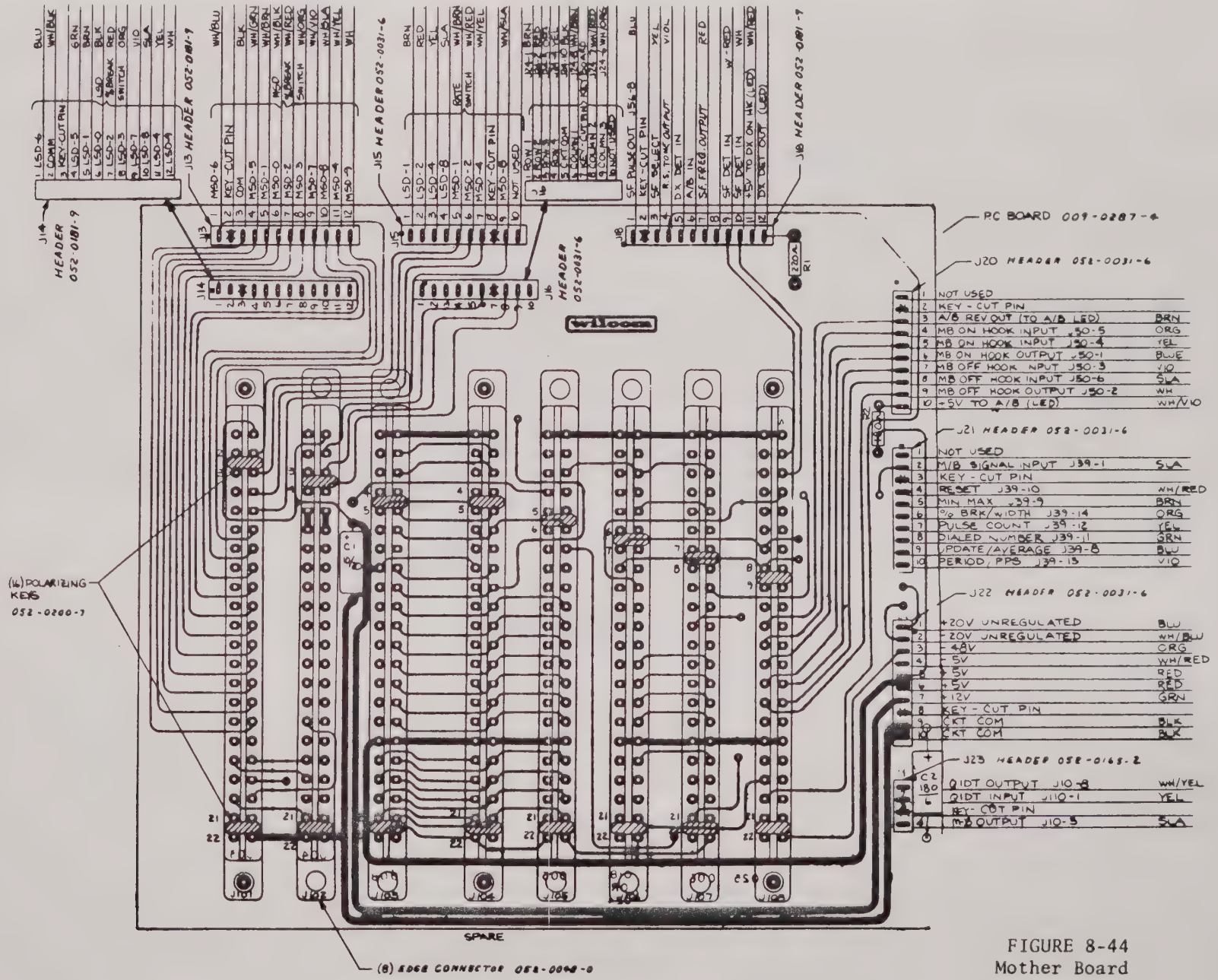


FIGURE 8-44
Mother Board
PC Assembly A28

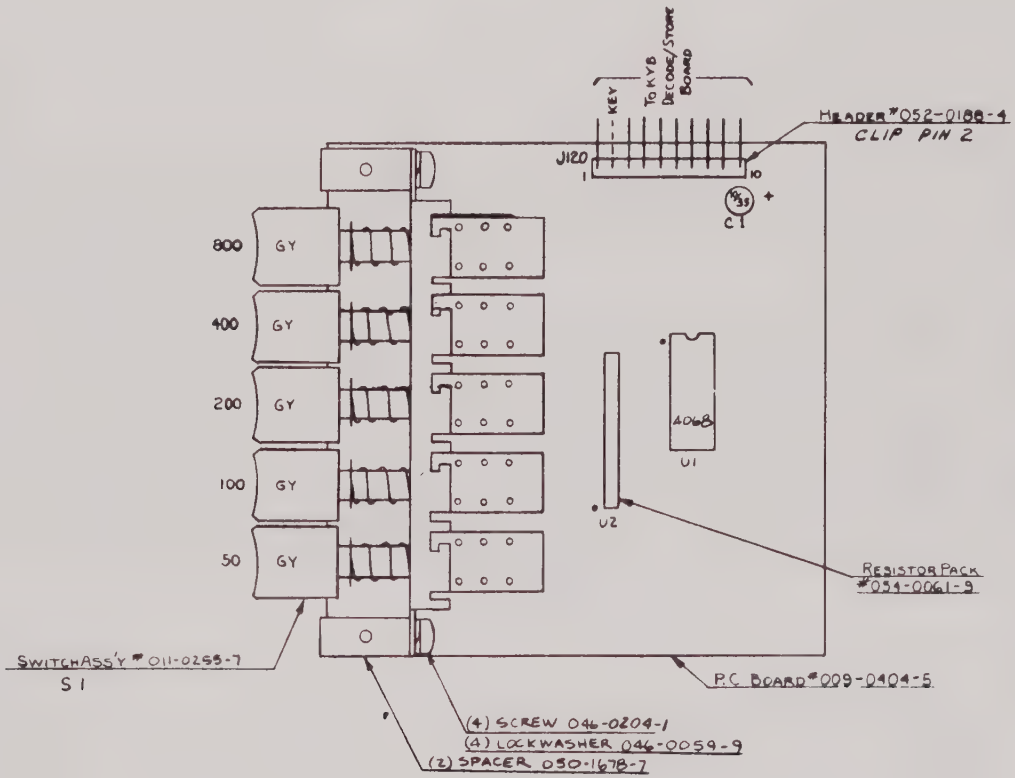


FIGURE 8-45
Interdigital Time Select
PC Assembly A29

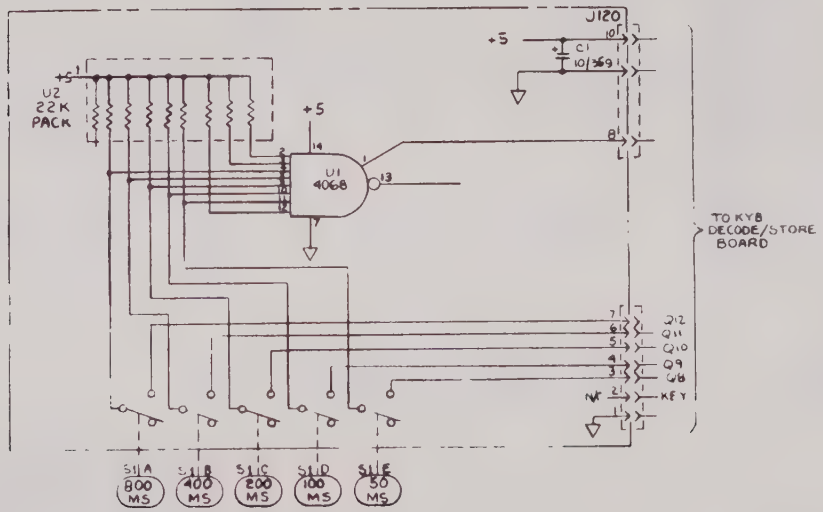


FIGURE 8-46
Interdigital Time Select
Schematic A29

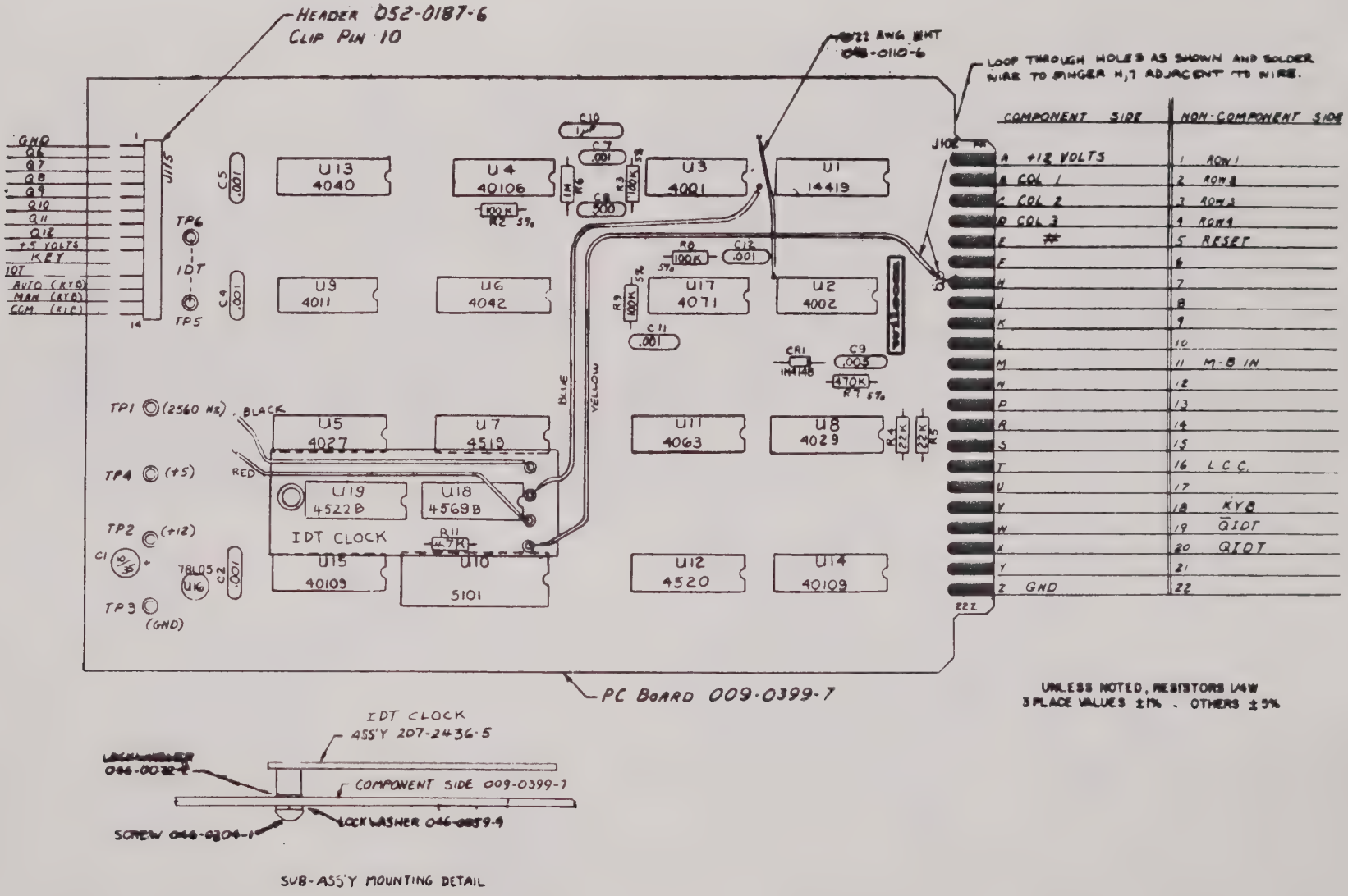
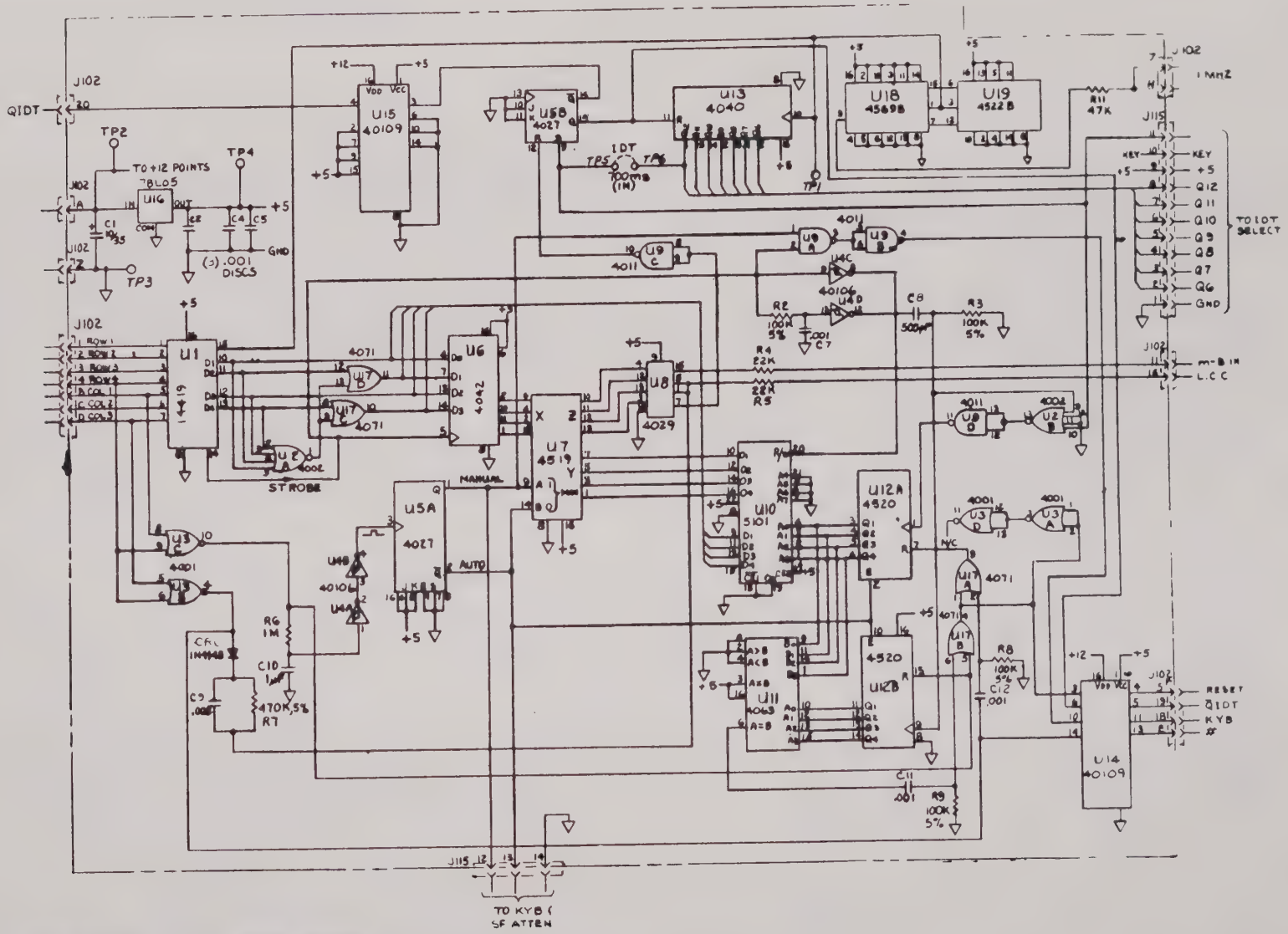


FIGURE 8-47
Keyboard-Decoder-Store Control
PC Assembly A30



UNUSED COMPONENT REFERENCE DESIGNATIONS		
U3A	U3D	U4C
U4E		

HIGHEST COMPONENT REFERENCE DESIGNATION		
R9	C12	CR6
U19		

UNLESS NOTED, RESISTORS ARE
3 PLACE VALUES ±1% OTHERS ±5%

FIGURE 8-48
Keyboard-Decoder-Store Control
Schematic A30

9.0 PARTS LIST

9.1 General

9.1.01 The Parts Lists provided on the following pages supply descriptions of the various assemblies, sub-assemblies and components that make up the Model T222C Signaling Test Set.

9.1.02 For those components purchased by Wilcom, the manufacturer and manufacturer's part number are provided. Those components manufactured by Wilcom are identified by a Wilcom part number.

9.1.03 Any required items may be ordered direct from Wilcom Products, Inc. or from the manufacturer.

T222C SIGNALING TEST SET - (30222046)

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	PORTABLE CASE SHELL ASS'Y	1	Wilcom	20008470
	PANEL COVER ASS'Y	1	Wilcom	20007845
A1	MAIN ASS'Y	1	Wilcom	20011037
	RUBBER, BUMPER, 5/8" HIGH	2	Russell	REC-2096S
	TILT STAND	1	Buckeye	MP4000810
	CORD SET, 3 COND (NEW STYLE) BLACK	1	Belden	17250

MAIN ASSEMBLY - (20011037) - A1

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
A2	FRONT PANEL ASS'Y	1	Wilcom	20010690
A3	CHASSIS BOX ASS'Y	1	Wilcom	20007878
A4	REAR ACCESS PANEL ASS'Y	1	Wilcom	20008421

FRONT PANEL ASSEMBLY - (20010690) - A2

Ref Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	FRONT PANEL	1	Wilcom	04408209
	PANEL (FOR OPTIONAL 3 F FREQUENCIES)	1	Wilcom	04411310
	PANEL DETAIL	Ref	Wilcom	04408191
	DISPLAY SYS. 32 CHAR.	1	Burroughs	SSD0132-0030
	WIRING HARNESS INSTALLATION #1	Ref	Wilcom	50006345
	JACK BLOCK ASSEMBLY, BUSING & WIRING	1	Wilcom	20007803
	HANDLE, 4" OC MOUNTING	2	Budradio	H-9111B
A14	PC ASS'Y, DX SUPERVISION	1	Wilcom	20007910
A13	PC ASS'Y, SF SUPERVISION CIRCUITS	1	Wilcom	20007928
A12	PC ASS'Y, E&M SUPERVISION	1	Wilcom	20007936
A11	PC ASS'Y, SEND INTERFACE CONTROL	1	Wilcom	20007944
A10	PC ASS'Y, DISPLAY CONTROL SWITCHING	1	Wilcom	20007985
A9	PC ASS'Y, LEAK COND & SF IMPEDANCE	1	Wilcom	20007993
A8	PC ASS'Y, LOOP RESIST & SEND CONTROL	1	Wilcom	20008017
A5	PC ASS'Y, RECEIVE PULSING TYPE	1	Wilcom	20008041
A6	PC ASS'Y, RECEIVE INTERFACE CONTROL	1	Wilcom	20010807
A7	PC ASS'Y, SEND PULSE TYPE CONTROL	1	Wilcom	20010815
A15	PC ASS'Y, KEYBOARD & S.F. ATTENUATOR	1	Wilcom	20010831
A29	PC ASS'Y, INTERDIGITAL TIME SELECT	1	Wilcom	20010898

A2 - CONTINUED

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	FUSE HOLDER	1	Littlefuse	348611
	FUSE HOLDER	1	Littlefuse	F348001
	FUSE, DUAL-SLOW: (1/4X1-1/4)	1	Bussman	MDL2
	TUBING, HEAT SHRINK, 3/4 DIA	A/R	Alpha	FIT 221-3/4"
	POWER SWITCH ASSEMBLY	1	Wilcom	20010864
	LED, Red	8	VisualComm	CLF280RTP
	LED, Green	2	VisualComm	CLF280GTP
	WIRING HARNESS INSTALLATION #2	Ref	Wilcom	50006352
	WIRING HARNESS ASSEMBLY, THUMBWHEEL	1	Wilcom	20010849
	WIRING HARNESS ASSEMBLY	1	Wilcom	20008397
	WIRING HARNESS, IDT SELECT	1	Wilcom	20010856
	WIRING HARNESS INSTALLATION #3	Ref	Wilcom	50006360
	DISPLAY WIRING ASSEMBLY	1	Wilcom	20007225
	WIRE HARNESS ASSEMBLY	1	Wilcom	20008405
	WIRE HARNESS ASSEMBLY	1	Wilcom	20008397
	WIRING HARNESS INSTALLATION #1	Ref	Wilcom	50006345

CHASSIS BOX ASSEMBLY - (20007878) - A3

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	CHASSIS BOX	1	Wilcom	04405726
	BRACKET, Chassis Box	2	Wilcom	04405775
A16	PC ASS'Y, 12 to 250 VOLT CONVERTER	1	Wilcom	20007274
A17	PC ASS'Y, LOOP & LINE PULSER	1	Wilcom	20007951
A18	PC ASS'Y, LOOP DETECTOR	1	Wilcom	20007266
	RIBBON CABLE ASS'Y	1	Wilcom	20007209
	INDUCTOR ASS'Y	2	Wilcom	20007258

REAR ACCESS PANEL ASSEMBLY - (20008421) - A4

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
A19	PC ASS'Y, POWER SUPPLY 115V/230V	1	Wilcom	20007837
	WIRING HARNESS ASS'Y, POWER SUPPLY	1	Wilcom	20008413
T1	TRANSFORMER POWER (6531)	1	Wilcom	04200937

A4 - CONTINUED

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	HINGE, REAR PANEL	1	Wilcom	04405767
	CARD CAGE ASS'Y	1	Wilcom	20724472
	BRACKET, POWER PLUG	1	Wilcom	04405783
	PANEL (REAR), (110/230)	1	Wilcom	04407623
	BRACKET CARD RETAINER	1	Wilcom	04405643
	BOOT (NEW STYLE)	1	Wilcom	05015771
	CORD RETAINER	1	Wilcom	04402962
U3,4	IC, Linear, Pos 5-Volt Reg, To-3	2	Nat'l Semi	LM323K
U5,6	IC, Linear, +12V +/-5% Reg, To-3	2	Nat'l Semi	LM7812CK
P61	HOUSING, PANEL MOUNT, 6 POS	1	AMP	1-480271-0
	CONTACT, MALE, 18-24 AWG	6	AMP	60618-4
S13	SWITCH SLIDE (LINE VOLTAGE SELECT)	1	Wilcom	01101245
	RECEPTACLE, POWER	1	Swcraft	EAC-301
	CLAMP, CAPACITOR:END MOUNT, I-3/8 DIA	3	Sprague	4586-97A
C12,13,14	CAPACITOR, ALUM ELECT: RADIAL, 30V 8000UF	3	CE CAP	86F547M
	SOCKET, POWER TRANSISTOR (To-3)	4	H H Smith	6266
	FAN: 4.71" SQ x 1.50", 115 VAC 50/60 HZ	1	Rotron	WR2A1
	FINGER GUARD, 4-½" FAN	1	Rotron	476042
	BUSHING STRAIN RELIEF	1	Heyco	SR3P4
	BINDING POST, (Black)	1	Grayhill	29-1 Blk
	CABLE ANCHOR, NYLON: ADHESIVE BACK	2	Panduit	ABMS-A
	WIRING HARNESS INSTALLATION	Ref	Wilcom	50009281

PC ASSEMBLY, RECEIVE PULSING TYPE - (20008041) - A5

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R2	RESISTOR, STABLE FILM: 1%, 4W 402 OHM	1	TRW/IRC	GS3
R1	RESISTOR, STABLE FILM: 1%, 4W 604 OHM	1	TRW/IRC	GS3
S2	SWITCH ASS'Y, Push Button	1	Wilcom	01102029
J14	MASS TERM HEADER, Right Angle 26 POS	1	3M Elex	3429-1002
J55	HEADER, Rt Angle Post, .100 OC, 8 POS	1	Molex	22-05-2081
J56	HEADER, Rt Angle Post, .100 OC, 10 POS	1	Molex	22-05-2101

PC ASSEMBLY, RECEIVE INTERFACE CONTROL - (20010807) - A6

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R1,2	RESISTOR, STABLE FILM: 1%, 4W 130 OHM	2	TRW/IRC	GS3

A6 - CONTINUED

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
S3	SWITCH ASSEMBLY, PUSH BUTTON	1	Wilcom	01102565
J51	HEADER, Rt Angle Post, .100 OC, 10 Pos	1	Molex	22-05-2101
J52	HEADER, Rt Angle Post, .100 OC, 12 Pos	1	Molex	22-05-2121
J53	MASS TERM HEADER, Rt Angle 26 Pos	1	3M Elex	3429-1002

PC ASSEMBLY, SEND PULSE TYPE CONTROL - (20010815) - A7

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R2	RESISTOR, STABLE FILM: 1%, 4W 402 ohm	1	TRW/IRC	GS3
R1	RESISTOR, STABLE FILM: 1%, 4W 604 ohm	1	TRW/IRC	GS3
R3	RESISTOR, WIREWOUND: 5%, 10W 150 ohm	1	Ohmite	20J150
S8	SWITCH ASS'Y, PUSH BUTTON	1	Wilcom	01102573
J29	HEADER, Rt Angle Post, .100 OC, 8 Pos	1	Molex	22-05-2081
J30	HEADER, Rt Angle Post, .100 OC, 12 Pos	1	Molex	22-05-2121
J31	MASS TERM HEADER, Rt Angle 26 Pos	1	3M Elex	3429-1002

PC ASSEMBLY, LOOP RESIST & SEND CONTROL (20008017) - A8

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R5,6,13, 14	RESISTOR, STABLE FILM: 1%, .75W 100 ohm	4	TRW/IRC	T060
R8,9,16, 17	RESISTOR, STABLE FILM: 1%, .75W 402 ohm	4	TRW/IRC	T060
R7,15	RESISTOR, STABLE FILM: 1%, 4W 100 ohm	2	TRW/IRC	GS3
R10,18	RESISTOR, STABLE FILM: 1%, 4W 402 ohm	2	TRW/IRC	GS3
R11,19	RESISTOR, STABLE FILM: 1%, 4W 806 ohm	2	TRW/IRC	GS3
R12,20	RESISTOR, STABLE FILM: 1%, 4W 1.62 k	2	TRW/IRC	GS3
R1,3	RESISTOR, STABLE FILM: 5%, .25W 470 ohm	2	TRW/IRC	RG1/4
R2,4	RESISTOR, STABLE FILM: 5%, .25W 47 k	2	TRW/IRC	RG1/4
Q1	TRANSISTOR, PNP AMPLIFIER	1	Moto Semi	MPS6523
Q2	TRANSISTOR, NPN AMPLIFIER	1	Moto Semi	MPS6521
J10,110	HEADER, Str Post, .100 OC, 8 Pos	2	AMP	87224-8
S9	SWITCH ASS'Y, PUSH BUTTON	1	Wilcom	01102094

PC ASSEMBLY, LEAK COND & SF IMPEDANCE - (20007993) - A9

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R7,14	RESISTOR, STABLE FILM: 1%, .25W 130 ohm	2	TRW/IRC	T055
R6,12	RESISTOR, STABLE FILM: 1%, .25W 274 ohm	2	TRW/IRC	T055
R5,13,16	RESISTOR, STABLE FILM: 1%, .25W 604 ohm	3	TRW/IRC	T055
R15	RESISTOR, STABLE FILM: 1%, .25W 4.42 k	1	TRW/IRC	T055
R17,18	RESISTOR, STABLE FILM: 1%, .25W 10.2 k	2	TRW/IRC	T055
R1,8	RESISTOR, STABLE FILM: 1%, 125W 13.3 k	2	TRW/IRC	T055
R20	RESISTOR, STABLE FILM: 1%, .25W 15.0 k	1	TRW/IRC	T055
R2,9	RESISTOR, STABLE FILM: 1%, .25W 15.8 k	2	TRW/IRC	T055
R19	RESISTOR, STABLE FILM: 1%, .25W 20.3 k	1	TRW/IRC	T055
R3,10	RESISTOR, STABLE FILM: 1%, .25W 64.9 k	2	TRW/IRC	T055
R4,11	POT, TRIM: RECT, 15T 200 ohm	2	Beck/Heli	89PR200
C1	CAPACITOR, AXIAL MPE: 5%, 200V 2.16 uF	1	F-Dyne	MPE21-2.16-200-5
T1,2	TRANSFORMER (SIGNAL OUTPUT) (TECO 5380)	2	Wilcom	04200275
U1	IC, Linear, Dual Gen Pur Op Amp	1	Moto Semi	MC1458P1
J11	HEADER, Str Post, .100 OC, 14 Pos	1	AMP	1-87224-4
S10	SWITCH ASS'Y, PUSH BUTTON	1	Wilcom	01102102

PC ASSEMBLY, DISPLAY CONTROL SWITCHING - (20007985) - A10

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R1	RESISTOR, STABLE FILM: 5%, .25W 270 ohm	1	TRW/IRC	RG1/4
R6,11	RESISTOR, STABLE FILM: 5%, .25W 1 k	2	TRW/IRC	RG1/4
R12,13	RESISTOR, STABLE FILM: 5%, .25W 2.2 k	2	TRW/IRC	RG1/4
R2,4,5,7,8	RESISTOR, STABLE FILM: 5%, .25W 4.7 k	5	TRW/IRC	RG1/4
R14	RESISTOR, STABLE FILM: 5%, .25W 10 k	1	TRW/IRC	RG1/4
R9	RESISTOR, STABLE FILM: 5%, .25W 560 k	1	TRW/IRC	RG1/4
R10,3	RESISTOR, STABLE FILM: 5%, .25W 22 k	2	TRW/IRC	RG1/4
C1	CAPACITOR, TANT ELECT: DIP RAD, 10%, 35V 1.0 uF	1	Sprague	199D105X9035BG2
C2	CAPACITOR, TANT ELECT: AXIAL, 10%, 35V 3.3 uF	1	Sprague	150D335X903582
CR1	DIODE, Signal	1	Ge Semi	1N4148
Q1,2	TRANSISTOR, NPN AMPLIFIER	2	Moto Semi	MPS6521
	SWITCH ASS'Y, PUSH BUTTON	1	Wilcom	01102011
DS1	LED, Red Point Source, T1-3/4 Cyl	1	Monsanto	MV5053
U1	IC, TTL, DUAL RETRIGGERABLE MONO	1	Nat'l Semi	DM8853N
U2	IC, TTL, QUAD D-TYPE FLIP-FLOP	1	Ti Semi	SN74175N
J39	HEADER, Str Post, .100 OC, 14 Pos	1	AMP	1-87224-4

PC ASSEMBLY, SEND INTERFACE CONTROL - (20007944) - A11

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	SWITCH ASSEMBLY, PUSH BUTTON	1	Wilcom	01102078
	HEADER, Rt Angle Post, .100 OC, 8 Pos	1	Molex	22-05-2081
J32	HEADER, Rt Angle Post, .100 OC, 14 Pos	1	Molex	22-05-2141
J34	MASS TERM HEADER, Rt Angle 26 Pos	1	3M Elex	3429-1002

PC ASSEMBLY, E&M SUPERVISION - (20007936) - A12

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
S4	SWITCH ASS'Y, PUSH BUTTON	1	Wilcom	01102045
R1,18	RESISTOR W W: 5%, 10W, 470 ohm	2	Tel Labs	EL10A
R6,25	RESISTOR, STABLE FILM: 5%, .25W 270 ohm	2	TRW/IRC	RG1/4
R2,19,12	RESISTOR, STABLE FILM: 5%, .25W 4.7 k	3	TRW/IRC	RG1/4
R5,7,24,26, 27,10	RESISTOR, STABLE FILM: 5%, .25W 10 k	6	TRW/IRC	RG1/4
R8	RESISTOR, STABLE FILM: 5%, .25W 15 k	1	TRW/IRC	RG1/4
R3,13,15, 16,21,23	RESISTOR, STABLE FILM: 5%, .25W 47 k	6	TRW/IRC	RG1/4
R9	RESISTOR, STABLE FILM: 5%, .25W 100 k	1	TRW/IRC	RG1/4
R11	RESISTOR, STABLE FILM: 5%, .25W 150 k	1	TRW/IRC	RG1/4
R4	RESISTOR, STABLE FILM: 5%, .25W 330 k	1	TRW/IRC	RG1/4
R14,17,20 22	RESISTOR, STABLE FILM: 5%, .25W 470 k	4	TRW/IRC	RG1/4
VR1	DIODE, Zener, 10V ±10%	1	Moto Semi	1N5240
VR2	DIODE, Zener, 3.3V ±5%	1	Moto Semi	1N5226B
C1	CAPACITOR, TANT ELECT: DIP RAD, 10%, 35V 10 uF	1	ITT	TAP-F10K35
Q1,4,6,9	TRANSISTOR, NPN High Voltage	4	Fchildsemi	2N5831
Q2,3,7,10	TRANSISTOR, NPN Low Noise	4	Fchildsemi	2N5961
Q5,8	TRANSISTOR, PNP High Voltage	2	Moto Semi	2N5401
CR1,2	DIODE, Signal	2	Ge Semi	1N4148
J38	HEADER, Str Post, .100 OC, 8 Pos	1	AMP	87224-8
J35,36,37	HEADER, Str Post, .100 OC, 6 Pos	3	AMP	87224-6

PC ASSEMBLY, SF SUPERVISION CIRCUITS - (20007928) -·A13

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer Number
	PC BOARD, SF SUPERVISION CKTS	1	Wilcom	00902890
R6,7	RESISTOR, STABLE FILM: 1%, .25W 604 ohm	2	TRW/IRC	T055
R3,4,5	RESISTOR, STABLE FILM: 5%, .25W 220 ohm	3	TRW/IRC	RG1/4
R1,2	RESISTOR, STABLE FILM: 5%, .25W 47 k	2	TRW/IRC	RG1/4
C5,6	CAPACITOR, AXIAL MPE: 10% 250V, 2 mF	2	INOCO	2LUMZ250
C1,2,3,4	CAPACITOR, ALUM ELECT: AXIAL, 350V 20 uF	4	CDE	WBR20-350
C7,8	CAPACITOR, TANT ELECT: DIP RAD, 10% 35V 10 uF	2	ITT	TAP-F10K35
U1	IC, CMOS, QUAD ANALOG TRANSMISSION GATE	1	Siliconix	DG201CJ
S5	SWITCH ASS'Y. PUSH BUTTON	1	Wilcom	01102052
J43	HEADER, STR POST, .100 OC, 8 Pos	1	AMP	87224-8
J44	HEADER, STR POST, .100 OC, 10 Pos	1	AMP	1-87224-2
J45	HEADER, STR POST, .100 OC, 12 Pos	1	AMP	1-87224-0

PC ASSEMBLY, DX SUPERVISION - (20007910) - A14

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
S6	SWITCH ASSEMBLY, PUSH BUTTON	1	Wilcom	01102060
R19,33	RESISTOR, STABLE FILM: 5%, .25W 270 ohm	2	TRW/IRC	RG1/4
R14,20,22	RESISTOR, STABLE FILM: 5%, .25W 1.5 k	3	TRW/IRC	RG1/4
R4,17	RESISTOR, STABLE FILM: 5%, .25W 2.2 k	2	TRW/IRC	RG1/4
R13	RESISTOR, STABLE FILM: 5%, .25W 4.7 k	1	TRW/IRC	RG1/4
R6,27	RESISTOR, STABLE FILM: 5%, .25W 6.8 k	2	TRW/IRC	RG1/4
R8,12,18, 26,32	RESISTOR, STABLE FILM: 5%, .25W 10 k	5	TRW/IRC	RG1/4
R3,9,11, 15,21,7, 25	RESISTOR, STABLE FILM: 5%, .25W 22 k	7	TRW/IRC	RG1/4
R28	RESISTOR, STABLE FILM: 5%, .25W 47 k	1	TRW/IRC	RG1/4
R5,24	RESISTOR, STABLE FILM: 5%, .25W 100 k	2	TRW/IRC	RG1/4
R10	RESISTOR, STABLE FILM: 5%, .25W 150 k	1	TRW/IRC	RG1/4
R16	RESISTOR, STABLE FILM: 1%, .25W 4.02 k	1	TRW/IRC	T055
R23	RESISTOR, STABLE FILM: 1%, .25W 6.04 k	1	TRW/IRC	T055
R29	RESISTOR, STABLE FILM: 1%, 4W 249 ohm	1	TRW/IRC	GS3
R1,2,30,31	RESISTOR, STABLE FILM: 1%, 4W 365 ohm	4	TRW/IRC	GS3
C1,2	CAPACITOR, TANT ELECT: 10%, 35V 10 uF	2	ITT COMPON	TAP-F10k35
Q3,8,10	TRANSISTOR, NPN HIGH VOLTAGE	3	FCHILDSEMI	2N5831
Q1,6,9,11	TRANSISTOR, PNP HIGH VOLTAGE	4	Moto Semi	2N5401
Q2,4,5,7, 12	TRANSISTOR, NPN LOW NOISE	5	FCHILDSEMI	2N5961
CR2,4,7-9, 11,12	DIODE, Signal	8	Ge Semi	1N4148
CR1,3,5,6, 10,13	DIODE, Rectifier, 1A	6	Moto Semi	1N4005
U1,2	IC, Optoelect, LED & NPN XSTR Opto-Isolator	2	Ge Semi	4N35
J46	HEADER, Str Post, .100 OC, 6 Pos	1	AMP	87224-6
J47	HEADER, Str Post, .100 OC, 8 Pos	1	AMP	87224-8
J48	HEADER, Str Post, .100 OC, 12 Pos	1	AMP	1-87224-2

PC ASSEMBLY, KEYBOARD & S.F. ATTENUATOR - (20010831) - A15

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R11	RESISTOR, STABLE FILM: 1%, .25W 412 ohm	1	TRW/IRC	T055
R10	RESISTOR, STABLE FILM: 1%, .25W 453 ohm	1	TRW/IRC	T055
R9	RESISTOR, STABLE FILM: 1%, .25W 511 ohm	1	TRW/IRC	T055
R8	RESISTOR, STABLE FILM: 1%, .25W 604 ohm	1	TRW/IRC	T055
R7	RESISTOR, STABLE FILM: 1%, .25W 665 ohm	1	TRW/IRC	T055
R6	RESISTOR, STABLE FILM: 1%, .25W 750 ohm	1	TRW/IRC	T055
R5	RESISTOR, STABLE FILM: 1%, .25W 866 ohm	1	TRW/IRC	T055
R4	RESISTOR, STABLE FILM: 1%, .25W 976 ohm	1	TRW/IRC	T055
R3	RESISTOR, STABLE FILM: 1%, .25W 1.07 k	1	TRW/IRC	T055
R1	RESISTOR, STABLE FILM: 1%, .25W 2.00 k	1	TRW/IRC	T055
R16	RESISTOR, STABLE FILM: 1%, .25W 3.16 k	1	TRW/IRC	T055
R12	RESISTOR, STABLE FILM: 1%, .25W 3.48 k	1	TRW/IRC	T055
R15	RESISTOR, STABLE FILM: 1%, .25W 6.81 k	1	TRW/IRC	T055

A15 - CONTINUED

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R2	RESISTOR, STABLE FILM: 1%, .25W 20.0 k	1	TRW/IRC	T055
R14	RESISTOR, STABLE FILM: 1%, .25W 21.5 k	1	TRW/IRC	T055
R13	RESISTOR, STABLE FILM: 1%, .25W 68.1 k	1	TRW/IRC	T055
R17,18	RESISTOR, STABLE FILM: 5%, .25W 470 ohm	2	TRW/IRC	RG1/4
R19,20	RESISTOR, STABLE FILM: 5%, .25W 22 k	2	TRW/IRC	RG1/4
DS1,3,4	LED, Red Point Source, T 1-3/4 Cyl	3	Monsanto	MV5053
DS2	LED, Grn Diffused T1-3/4 Cyl	1	Monsanto	MV5254
C1	CAPACITOR, DISC: 10%, 500V, x5F .001 uF	1	Erie Tech	801-000 X5F0 102K
C2,3	CAPACITOR, TANT ELECT: Dip Rad, 10%, 35V 10 uF	2	ITT Compon	TAP-F10K35
CR1-24	DIODE, Signal	24	Ge Semi	1N4148
Q1,2	TRANSISTOR, NPN Amplifier	2	Moto Semi	MPS6521
U1	IC, Linear, Dual Gen Pur Op Amp	1	Moto Semi	MC1458P1
S1	DIAL PAD	1	Clare-Pend	940002
J28,117	HEADER, Str Post, .100 OC, 4 Pos	2	AMP	87224-4
J25,26,116	HEADER, Str Post, .100 OC, 6 Pos	3	AMP	87224-6
J24,27	HEADER, Str Post, .100 OC, 12 Pos	2	AMP	1-87224-2

PC ASSEMBLY, 12 TO 250 VOLT CONVERTER - (20007274) - A16

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R3	RESISTOR, STABLE FILM: 5%, .25W 470 ohm	1	TRW/IRC	RG1/4
R4	RESISTOR, STABLE FILM: 5%, .25W 1.2 k	1	TRW/IRC	RG1/4
R2	RESISTOR, STABLE FILM: 5%, .25W 10 k	1	TRW/IRC	RG1/4
R1	RESISTOR, STABLE FILM: 5%, .25W 18 k	1	TRW/IRC	RG1/4
R5	RESISTOR, STABLE FILM: 5%, .25W 3 Meg	1	TRW/IRC	RG1/4
C1	CAPACITOR, ALUM ELECT: AXIAL, 25V 100 uF	1	Sprague	TE-1211
C2	CAPACITOR, RADIAL PE: 10%, 100V .022 uF	1	Sprague	225P2239IWD3
C3	CAPACITOR, MONO: 20%, 50V, Z5U .10 uF	1	Sprague	7CZ5U104X005001
U1	IC, CMOS, DUAL RETRIGGERABLE MONO	1	Moto Semi	MC145288CP
U2	POWER SUPPLY	1	Endicott	E912
Q1	TRANSISTOR, NPN AMPLIFIER	1	Moto Semi	MPS6521
Q2	TRANSISTOR, PNP POWER	1	Moto Semi	2N4918
L1	INDUCTOR, AXIAL, 10% 4.7 uF	1	Cambion	550-2960-36-02-00
J65	HEADER, Str Post, .100 OC, 6 Pos	1	AMP	87224-6
J66	HEADER, Str Post, .100 OC, 14 Pos	1	AMP	1-87224-4
J67	MASS TERM HEADER, Rt Angle 26 Pos	1	3M Elex	3429-1002

PC ASSEMBLY, LOOP & LINE PULSER - (20007951) - A17

Ref. Design.	Description		Qty.	Mfr.	Manufacturer's Number
R21,22	RESISTOR, STABLE FILM: 1%, .25W	8.25 ohm	2	TRW/IRC	TF07
R5	RESISTOR, STABLE FILM: 1%, 4W	1.62 k	1	TRW/IRC	GS3
R57,58,78, 82,54,36	RESISTOR, STABLE FILM: 5%, .25W	4.7 ohm	6	TRW/IRC	TF07
R52,80	RESISTOR, STABLE FILM: 5%, .25W	330 ohm	2	TRW/IRC	RG1/4
R60	RESISTOR, STABLE FILM: 5%, .25W	470 ohm	1	TRW/IRC	RG1/4
R53,59,81	RESISTOR, STABLE FILM: 5%, .25W	680 ohm	3	TRW/IRC	RG1/4
R7,8,29 30,37,38, 50,56,79, 77	RESISTOR, STABLE FILM: 5%, .25W	1 k	10	TRW/IRC	RG1/4
R48,75	RESISTOR, STABLE FILM: 5%, .25W	1.5 k	2	TRW/IRC	RG1/4
R27,35	RESISTOR, STABLE FILM: 5%, .25W	1.8 k	2	TRW/IRC	RG1/4
R25	RESISTOR, STABLE FILM: 5%, .25W	2.2 k	1	TRW/IRC	RG1/4
R10,23,44, 47,49,51, 55,63,67,71	RESISTOR, STABLE FILM: 5%, .25W	4.7 k	10	TRW/IRC	RG1/4
R26,34,46, 65,72	RESISTOR, STABLE FILM: 5%, .25W	6.8 k	5	TRW/IRC	RG1/4
R15,18,31, 39	RESISTOR, STABLE FILM: 5%, .25W	8.2 k	4	TRW/IRC	RG1/4
R1,3,11,14 42,43,61, 62,68,69	RESISTOR, STABLE FILM: 5%, .25W	10 k	10	TRW/IRC	RG1/4
R33,41	RESISTOR, STABLE FILM: 5%, .25W	22 k	2	TRW/IRC	RG1/4
R2,6,12 16	RESISTOR, STABLE FILM: 5%, .25W	47 k	4	TRW/IRC	RG1/4
R4,13,17, 45,64,70	RESISTOR, STABLE FILM: 5%, .25W	100 k	6	TRW/IRC	RG1/4
R21,22	RESISTOR, STABLE FILM: 1%, .25W	8.25 ohm	2	TRW/IRC	TF07
R9,28	RESISTOR, CARBON: 5%, .5W	6.2 ohm	2	A-B	EB
R66	RESISTOR, CARBON: 5%, .5W	15 k	1	A-B	FB ½W 5% RESIS
R5	RESISTOR, STABLE FILM: 1 %, 4W	1.62 k	1	TRW/IRC	GS3
R19,20	RESISTOR, WIREWOUND: 5%, 10 W	150 ohm	2	Ohmite	20J150
R32,40	POT, TRIM: rect, 15T	10 k	2	Beck/Heli	89PR10K
C1,2	CAPACITOR, Disc: 10%, 500V, Z5U	0.01 uF	2	Erie Tech	811-000 Z5UO 103M
Q4,23,33	TRANSISTOR, NPN Power		3	Moto Semi	MJE340
Q11,14,18, 27,34	TRANSISTOR, PNP Power		5	Moto Semi	MJE350
Q21,31	TRANSISTOR, PNP Low Noise		2	Fchildsemi	2N4249
Q1,2,6,9 12,13,29, 15-17,19, 22,25,28	TRANSISTOR, PNP High Voltage		16	Moto Semi	2N5401
Q7,8,10, 20,26,30	TRANSISTOR, NPN High Voltage		6	FCHILDSEMI	2N5831

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Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
Q3,5,24	TRANSISTOR, NPN Low Noise	3	Fchildsemi	2N5961
CR1-8	DIODE, Rectifier, 1A	8	Moto Semi	1N4005
VR1,2	DIODE, Zener, 33V +-10%	2	Moto Semi	1N5257A
U1	IC, Optoelect, LED/NPN-XSTR Isolator	1	Ge Semi	H11D1
	HEADER, Str Post, .100 OC, 10 Pos	1	AMP	1-87224-0
	HEADER, Str Post, .100 OC, 12 Pos	1	AMP	1-87224-2
	HEAT SINK, Pulser Front	1	Wilcom	04405676

PC BOARD ASSEMBLY, LOOP DETECTOR - (20007266) - A18

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	STANDOFF, Swage; ¼Rnd 3/16 L	4	Rush Ind	9532B-B-0632-28
R4,6,18, 20	RESISTOR, STABLE FILM: 1%, .25W 20.0 k	4	TRW/IRC	T055
R2,9,11, 16,21,23	RESISTOR, STABLE FILM: 1%, .25W 49.9 k	6	TRW/IRC	T055
R1,8,12, 13,15	RESISTOR, STABLE FILM: 1%, .25W 100 k	5	TRW/IRC	T055
R3,10, 17,22	RESISTOR, STABLE FILM: 1%, .25W 249 k	4	TRW/IRC	T055
R37	RESISTOR, STABLE FILM: 1%, .25W 13.3 k	1	TRW/IRC	T055
R7,14	RESISTOR, STABLE FILM: 1%, 4W 69.8 ohm	2	TRW/IRC	GS3
R48	RESISTOR, STABLE FILM: 5%, .25W 1.5 k	1	TRW/IRC	RG1/4
R53,54, 55	RESISTOR, STABLE FILM: 5%, .25W 2.2 k	3	TRW/IRC	RG1/4
R45,46	RESISTOR, STABLE FILM: 5%, .25W 3.3 k	2	TRW/IRC	RG1/4
R27,31, 49	RESISTOR, STABLE FILM: 5%, .25W 4.7 k	3	TRW/IRC	RG1/4
R28,41	RESISTOR, STABLE FILM: 5%, .25W 8.2 k	2	TRW/IRC	RG1/4
R25,33, 40,52	RESISTOR, STABLE FILM: 5%, .25W 10 k	4	TRW/IRC	RG1/4
R43	RESISTOR, STABLE FILM: 5%, .25W 12 k	1	TRW/IRC	RG1/4
R30,50	RESISTOR, STABLE FILM: 5%, .25W 15 k	2	TRW/IRC	RG1/4
R38	RESISTOR, STABLE FILM: 5%, .25W 18 k	1	TRW/IRC	RG1/4
R24	RESISTOR, STABLE FILM: 5%, .25W 20 k	1	TRW/IRC	RG1/4
R32,51	RESISTOR, STABLE FILM: 5%, .25W 22 k	2	TRW/IRC	RG1/4
R34,36	RESISTOR, STABLE FILM: 5%, .25W 47 k	2	TRW/IRC	RG1/4
R42	RESISTOR, STABLE FILM: 5%, .25W 56 k	1	TRW/IRC	RG1/4
R39	RESISTOR, STABLE FILM: 5%, .25W 68 k	1	TRW/IRC	RG1/4
R26	RESISTOR, STABLE FILM: 5%, .25W 75 k	1	TRW/IRC	RG1/4
R35	RESISTOR, STABLE FILM: 5%, .25W 150 k	1	TRW/IRC	RG1/4

A18 - CONTINUED

Ref. Desig.	Description		Qty.	Mfr.	Manufacturer's Number
R44	RESISTOR, STABLE FILM: 5%, .25W	470 k	1	TRW/IRC	RG1/4
R29	POT, TRIM; Rect, 15T	10 k	1	Beck/Heli	89PR10K
R5,19,47	POT, TRIM; 15T, .75W	5 k	3	Bourns	89PR5K
C1,2	CAPACITOR, MONO: 20%, 50V, Z5U	1.0 uF	2	Sprague	7CZ5U105X0050E2
C3,4,6	CAPACITOR, TANT ELECT: Dip Rad, 10%, 35V	10 uF	3	ITT Compon	TAP-F10K35
C5	CAPACITOR, MONO: 20%, 50V, Z5U	1.0 uF	1	Sprague	7CZ5U105X0050E2
CR 1-4, 9,10	DIODE, Signal		6	Ge Semi	1N4148
CR5-8	DIODE, Rectifier, 1A		4	Moto Semi	1N4005
VR1	DIODE, Zener, 15V ±10%		1	Moto Semi	1N5245A
Q1-4	TRANSISTOR, NPN Low Noise		4	Fchildsemi	2N5961
Q5	TRANSISTOR, PNP Power		1	Moto Semi	MJE350
U1,2, 3,4	IC, Linear, Dual Op Amp		4	Signetics	NE532N
U5	IC, Linear, -24V ±5% Reg. to -39		1	Nat'l Semi	LM320H-24
J57	HEADER, Str Post, .100 OC, 12 Pos		1	AMP	1-87224-2
JL1,2	HEADER, Str Post, .100 OC, 4 Pos		2	AMP	87224-4
J58	HEADER, Str Post, .100 OC, 6 Pos		1	AMP	87224-6

PC ASSEMBLY, POWER SUPPLY 115V/240V - (20007837) - A19

Ref. Desig.	Description		Qty.	Mfr.	Manufacturer's Number
C1	CAPACITOR, ALUM ELECT: Axial, 100V	780 uF	1	Sprague	39D787F100JT4
C2	CAPACITOR, ALUM ELECT: Axial, 50V	1100 uF	1	Ge Cap	8HF229ANA
C3	CAPACITOR, ALUM ELECT: Axial, 75V	1000 uF	1	Sprague	39D108G075JP4
C4,5, 6,7	CAPACITOR, TANT ELECT: Axial, 10%, 20V	100 uF	4	Sprague	150D107X9020S2
C8,9, 10,11	CAPACITOR, MONO: 20%, 50V, Z5U	1.0 uF	4	Sprague	7CZ5U105X0050E2
CR1,2, 3,4	DIODE, Rectifier, 1A		4	Moto Semi	1N4005
CR5-12	DIODE, Rectifier, 3A		8	Cramer El	1N5406
U1	IC, Linear, Neg 12-Volt Reg, to -220		1	Nat'l Semi	LM320T-12
U2	IC, Linear, Neg 5.2-Volt Reg, to -220		1	Nat'l Semi	LM320T-5.2
J1,3, 5,6	HEADER, Str Post, .100 OC, 14 Pos		4	AMP	1-87224-4
J2,4,7	HEADER, Str Post, .100 OC, 6 Pos		3	AMP	87224-6
J8,9	HEADER, Str Post, .100 OC, 8 Pos		2	AMP	87224-8

CARD CAGE ASSEMBLY - (20724472) - A20

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	BRACKET, CARD CAGE, Left	1	Wilcom	04405734
	BRACKET, CARD CAGE, Right	1	Wilcom	04405791
A28	PC ASSEMBLY, Mother Board	1	Wilcom	20008009
A21	PC ASSY, RATE & BREAK GENERATOR	1	Wilcom	20010880
A30	PC ASSY, KYB DECODER-STORE-CONTROL	1	Wilcom	20010773
A23	PC ASSY, INT TIMER & SELFSCAN INTERFACE	1	Wilcom	20009841
A24	PC ASSEMBLY, DATA INPUT CONTROL	1	Wilcom	20010948
A25	PC ASSEMBLY, CPU	1	Wilcom	20010799
A26	PC ASSY, A/D CONVERTER & FREQ. DIVIDER	1	Wilcom	20010823
A27	PC ASSY SF SEND-RECEIVE DETECTORS	1	Wilcom	20010906
	UPPER CARD GUIDE, ASSY	1	Wilcom	20007233
	LOWER CARD GUIDE, ASSY	1	Wilcom	20007241

PC ASSY, RATE & BREAK GENERATOR-(20010880) - A21

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R13	RESISTOR, Stable Film: 5%, .25W 3.3 k	1	TRW/IRC	RG1/4
R1-12	RESISTOR, Stable Film: 5%, .25W 10 k	12	TRW/IRC	RG1/4
C1	CAPACITOR, Dip Tant: 10%, 35V 10 uF	1	ITT	TAP-F10K35
C2	CAPACITOR, Disc: 10%, 500V, X5F 150 pF	1	ERIE	831-000-X5F0 151K
CR1-4	DIODE, Signal	4	G.E.	1N4148
U3,4	IC, Cmos, BCD Rate Multiplier	2	Motorola	MC14527BCP
U5-8	IC, Cmos, Decade Counter	4	RCA	CD4017BE
U9	IC, Cmos, Quad 2-Input Nor Gate	1	RCA	CD4001BE
U10,12	IC, Cmos, Dual D Flip-Flop	2	RCA	CD4013BE
U11	IC, Cmos, Quad 2-Input or Gate	1	RCA	CD4071BE
U13	IC, Cmos, Quad 2-Input and Gate	1	RCA	CD4081BE

— (NO A22) —

PC ASSEMBLY, INT TIMER & SELFSCAN INTERFACE - (20009841) - A23

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R8,10-15,17	RESISTOR, Stable Film: 5%, .25W 1 k	8	TRW/IRC	RG1/4
R7	RESISTOR, Stable Film: 5%, .25W 1.2 k	1	TRW/IRC	RG1/4
R1	RESISTOR, Stable Film: 5%, .25W 1.5 k	1	TRW/IRC	RG1/4
R3	RESISTOR, Stable Film: 5%, .25W 2.2 k	1	TRW/IRC	RG1/4

A23 - CONTINUED -

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R16	RESISTOR, Stable Film: 5%, .25W 2.7 k	1	TRW/IRC	RG1/4
R2	RESISTOR, Stable Film: 5%, .25W 6.8 k	1	TRW/IRC	RG1/4
R4,5, 6,18	RESISTOR, Stable Film: 5%, .25W 10 k	4	TRW/IRC	RG1/4
R9	RESISTOR, Stable Film: 5%, .25W 22 k	1	TRW/IRC	RG1/4
C4	CAPACITOR, Disc: 5%, 500V N750 56 pF	1	ERIE	801-000 U2J0 560J
C1,2 5,6	CAPACITOR, Disc: 10%, 500V, X5F .001 uF	4	ERIE	801-000 X5F0 102K
C3	CAPACITOR, Radial Pe: 10%, 100V .01 uF	1	Sprague	225P1039-1WD3
C7	CAPACITOR, Stack MPC: 55, 100V 47 uF	1	Siemens	532541
C8	CAPACITOR, Tant Elect; Dip Rad, 10%, 35V 10 uF	1	ITT	TAP-F10K35
Q1,2,3	TRANSISTOR, NPN Amplifier	3	Moto Semi	MPS6521
U1,10	IC, Lsttl, Octal Buffer, 3-State	2	Nat'l Semi	DM81LS95N
U2,12	IC, Cmos, Dual 4-Bit Binary Up Counter	2	Moto Semi	MC145208CP
U3,5,15	IC, Cmos, Dual J-K Flip-Flop	3	RCA	CD4027BE
U4,9	IC, Cmos, Quad 2-Input Nand Gate	2	RCA	CD4011BE
U6	IC, Lsttl, Hex D Flip-Flop	1	Signetics	N74LS174N
U7	IC, Cmos, Quad 2-Input or Gate	1	RCA	CD4071BE
U8	IC, Cmos, Quad 2-Input and Gate	1	RCA	CD4081BE
U11	IC, Ttl, Dual Retriggerable Mono	1	Nat'l Semi	DM8853N
U13, 14	IC, Cmos, Dual BCD Up Counter	2	Moto Semi	MC14518BCP
U16	IC, Lsttl, Quad D Flip-Flop	1	Ti Semi	SN74LS175N
J2	MASS TERM HEADER, Rt Angle 26 Pos	1	3M Elex	3429-1002

PC ASSY, DATA INPUT CONTROL - (20010948) - A24

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R1,2	RESISTOR, Stable Film: 5%, .25W 1 k	2	TRW/IRC	RG1/4
R3	RESISTOR, Stable Film: 5%, .25W 10 k	1	TRW/IRC	RG1/4
C1,2	CAPACITOR, Disc: 10%, 500V, X5F .001 uF	2	ERIE	801-000 X5F0 102K
C3,4,5,6, 7,8,9	CAPACITOR, Disc: 10%, 500V, Z5U 0.01 uF	7	ERIE	811-000 Z5U0 103M
C10	CAPACITOR, Tant Elect: Axial, 10%, 35V 6.8 uF	1	Sprague	150D685X-903582
U1,3	IC, Cmos, Quad 2-Input Nand Gate	2	RCA	CD4011BE
U2	IC, Sttl: 1 of 8 Decoder	1	Nat'l Semi	DM74S138N
U4,5	IC, Cmos, Dual 4-Bit Binary Up Counter	2	Moto Semi	MC14520BCP
U6,7,8,9	IC, Uproc, 8-Bit Input/Output Port	4	Intel	P8212
Q1	TRANSISTOR, NPN Amplifier	1	Moto Semi	MPS6521

PC ASSY, CPU - (20010799) - A25

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R3,4,5	RESISTOR, STABLE FILM: 5%, .25W 1 k	3	TRW/IRC	RG1/4
R1,2	RESISTOR, STABLE FILM: 5%, .25W 10 k	2	TRW/IRC	RG1/4
C1-9	CAPACITOR, MONO: 10%, 50V, Z5U 1.0 uF	9	Sprague	7CZ5U105X0050E2
C11-13	CAPACITOR, TANT ELECT: Dip Rad, 10%, 35V 10 uF	3	ITT	TAP-F10K35
C14	CAPACITOR, VARI, CERAMIC Rt Angle 7-25 pF	1	ERIE	538-0068-7-25
Y1	XTAL, 18.000 mHz 10 ohms 4.9 pF	1	Wilcom	05400064
U1	IC, Uproc, 8-Bit Microprocessor	1	Intel	D8080A
U2	IC, Uproc, Clock Generator for 8080A	1	Intel	P8224
U3	IC, Uproc, System Controller for 8080A	1	Intel	C8228
U4	IC, PROM 00700989, Pgm'd 50006337, T222C #1	1	Wilcom	00703405
	MADE FROM			
IC	Uproc, 1024 x 8 Mos Prom	Ref	Intel	C8708
	T222C SOURCE PROGRAM	Ref	Wilcom	50006337
U5	IC, PROM 00700989, Pgm'd 50006345, T222C #2	1	Wilcom	00703413
	MADE FROM			
	IC, Uproc, 1024 x 8 Mos Prom	Ref	Intel	C8708
	T222C SOURCE PROGRAM	Ref	Wilcom	50006337
U6	IC, PROM 00700989, Pgm'd 50006352, T222C #3	1	Wilcom	00703421
	IC, UPROC, 1024 x 8 Mos Prom	Ref	Intel	C8708
	T222C SOURCE PROGRAM	Ref	Wilcom	50006337
U7,8, 9,10	IC, MEMORY, 256 x 4 Static Mos Ram	4	Intel	P2111-1
U11	IC, LSTTL: Quad 2-Input and Gate	1	Signetics	N74LS08N
U12	IC, UPROC, 3-Bit Binary to 8-Line Decode	1	Intel	P8205
	SOCKET, DIP 40 Pin	1	TI	C934002
	SOCKET, DIP 28 Pin	1	TI	C932802
	SOCKET, DIP 24 Pin	3	TI	C932402
	SOCKET, DIP 18 Pin	4	TI	C931802
	BUS WIRE, 22 AWG	A/R		

PC ASSY, A/D CONVERTER & FREQ. DIVIDER - (20010823) - A26

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R7,10	RESISTOR, STABLE FILM: 1%, .25W 10.0 k	2	TRW/IRC	T055
R15	RESISTOR, STABLE FILM: 1%, .25W 12.1 k	1	TRW/IRC	T055
R3,5,6	RESISTOR, STABLE FILM: 1%, .25W 20.0 k	3	TRW/IRC	T055
R17	RESISTOR, STABLE FILM: 1%, .25W 316 k	1	TRW/IRC	T055
R18	RESISTOR, STABLE FILM: 5%, .25W 100 ohm	1	TRW/IRC	RG1/4
R23	RESISTOR, STABLE FILM: 5%, .25W 220 ohm	1	TRW/IRC	RG1/4
R24	RESISTOR, STABLE FILM: 5%, .25W 330 ohm	1	TRW/IRC	RG1/4
R11	RESISTOR, STABLE FILM: 5%, .25W 680 ohm	1	TRW/IRC	RG1/4
R22	RESISTOR, STABLE FILM: 5%, .25W 750 ohm	1	TRW/IRC	RG1/4

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R19,21	RESISTOR, STABLE FILM: 5%, .25W 1 k	2	TRW/IRC	RG1/4
R25,26	RESISTOR, STABLE FILM: 5%, .25W 4.7 k	2	TRW/IRC	RG1/4
R9	RESISTOR, STABLE FILM: 5%, .25W 6.8 k	1	TRW/IRC	RG1/4
R4	RESISTOR, STABLE FILM: 5%, .25W 15 k	1	TRW/IRC	RG1/4
R2	RESISTOR, STABLE FILM: 5%, .25W 20 k	k	TRW/IRC	RG1/4
R8	RESISTOR, STABLE FILM: 5%, .25W 47 k	1	TRW/IRC	RG1/4
R20	RESISTOR, STABLE FILM: 5%, .25W 100 k	1	TRW/IRC	RG1/4
R16	RESISTOR, STABLE FILM: 5%, .25W 1 meg	1	TRW/IRC	RG1/4
R12	POT, TRIM: RECT, 15T 1 k	1	Beck/Heli	89PR1K
R13,14	POT, TRIM: RECT, 15% 2 k	2	Beck/Heli	89PR2K
R1	POT, TRIM: RECT, 15T 20 k	1	Beck/Heli	89PR20K
C2	CAPACITOR, DISC: 5%, 500V, NPD 12 pF	1	ERIE	831-000 COGO 120J
C5	CAPACITOR, DISC: 5%, 500V, N750 68 pF	1	ERIE	851-000 U2JO 680J
C4	CAPACITOR, DISC: 10%, 500V, X5F 150 pF	1	ERIE	831-000 X5FO 151K
C6	CAPACITOR, DISC: 10%, 1000V, Z5F 300 pF	1	Centralab	DD-301
C13-19	CAPACITOR, DISC: 10%, 500V, Z5U 0.01 uF	7	ERIE	811-000 Z5UO 103M
C7,8	CAPACITOR, DISC: 10%, 50V, Z5U .10 uF	2	Sprague	7CZ5U104X0050D1
C1	CAPACITOR, MONO: 10%, 50V, Z5& 1.0 uF	1	Sprague	7CZ5U105X0050E2
C10,12	CAPACITOR, TANT ELECT: DIP RAD, 10%, 35V 1.0 uF	2	ITT	TAP-F1.0K35
C3,9.11, 20,21	CAPACITOR, TANT ELECT: DIP RAD, 10%, 35V 10 uF	5	ITT	TAP-F10K35
CR1-16	DIODE, SIGNAL	16	GE Semi	1N4148
CR1,2,-	DIODE, SIGNAL	A/R	GE Semi	1N4148
VR1	DIODE, TEMP COMP ZENER, 6.2V ±5%	1	Moto Semi	1N825
U1	IC, LINEAR, OP AMP, 741 TYPE	1	Moto Semi	MC1741CP1
U2	IC, LINEAR, DUAL GEN PUR OP AMP	1	Moto Semi	MC1458P1
U3	IC, LINEAR, LOGARITHMIC AMP	1	Intersil	8048BC
U4	IC, STTL: 1 of 8 DECODER	1	Nat'l Semi	DM74S138N
U4	IC, UPROC, 3-Bit Binary to 8-Line Decode	1	Intel	P8205
U6	IC, DATA CONV, 8-Bit Cmos A/D	1	Tdyne Semi	8700CN
U5,7	IC, LSTTL, DUAL J-K FLIP-FLOP	2	Signetics	N74LS107N
U8,9,15, 16,17	IC, LSTTL: SYNCHRONOUS 4-Bit Counter	5	Signetics	N74LS161AN
U10	RESISTOR NET, 10 Pin Sip 9 x 4.7 k ohm	1	CTS	750-101-R4.7K
U11	IC, LSTTL, OCTAL BUFFER, 3-State	1	Nat'l Semi	DM81LS95N
U12	IC, LINEAR, +12V ±5% Reg, to -92	1	Moto Semi	MC78L12ACP
U13	IC, LINEAR, Neg 12V ±5% Reg, to -92	1	Moto Semi	MC79L12ACP
U14	IC, LSTTL: QUAD 2-Input Nand Gate	1	Nat'l Semi	DM74LS00N
J121	HEADER, Rt Angle Post, .100 OC, 6 Pos	2	Molex	22-05-2061

PC ASSY, SF SEND-RECEIVE DETECTORS - (20010906) - A27

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R7,11	RESISTOR, STABLE FILM: 1%, .25W 2.61 k	2	TRW/IRC	T055
R56	RESISTOR, STABLE FILM: 1%, .25W 3.92 k	1	TRW/IRC	RN55D
R44	RESISTOR, STABLE FILM: 1%, .25W 4.12 k	1	TRW/IRC	TO55
R38	RESISTOR, STABLE FILM: 1%, .25W 4.99 k	1	TRW/IRC	T055
R37,41	RESISTOR, STABLE FILM: 1%, .25W 10.0 k	2	TRW/IRC	T055
R36	RESISTOR, STABLE FILM: 1%, .25W 12.4 k	1	TRW/IRC	T055
R34	RESISTOR, STABLE FILM: 1%, .25W 14.7 k	1	TRW/IRC	T055
R27,42	RESISTOR, STABLE FILM: 1%, .25W 15.0 k	2	TRW/IRC	T055
R39	RESISTOR, STABLE FILM: 1%, .25W 17.4 k	1	TRW/IRC	T055
R40	RESISTOR, STABLE FILM: 1%, .25W 17,8 k	1	TRW/IRC	T055
R2,4,6	RESISTOR, STABLE FILM: 1%, .25W 20.0 k	3	TRW/IRC	T055
R33	RESISTOR, STABLE FILM: 1%, .25W 21.5 k	1	TRW/IRC	T055
R35	RESISTOR, STABLE FILM: 1%, .25W 24.9 k	1	TRW/IRC	T055
R1,5	RESISTOR, STABLE FILM: 1%, .25W 49.9 k	2	TRW/IRC	T055
R12,18,31	RESISTOR, STABLE FILM: 1%, .25W 100 k	3	TRW/IRC	T055
R10	RESISTOR, STABLE FILM: 1%, .25W 130 k	1	TRW/IRC	T055
R19	RESISTOR, STABLE FILM: 1%, .25W 196 k	1	TRW/IRC	T055
R15,16,29	RESISTOR, STABLE FILM: 5%, .25W 1 k	3	TRW/IRC	RG1/4
R22,23	RESISTOR, STABLE FILM: 5%, .25W 1.5 k	2	TRW/IRC	RG1/4
R43	RESISTOR, STABLE FILM: 5%, .25W 2.7 k	1	TRW/IRC	RG1/4
R21	RESISTOR, STABLE FILM: 5%, .25W 3.9 k	1	TRW/IRC	RG1/4
R9,13,20, 25,54	RESISTOR, STABLE FILM: 5%, .25W 4.7 k	5	TRW/IRC	RG1/4
R28,32,53	RESISTOR, STABLE FILM: 5%, .25W 10 k	3	TRW/IRC	RG1/4
R30	RESISTOR, STABLE FILM: 5%, .25W 12 k	1	TRW/IRC	RG1/4
R14	RESISTOR, STABLE FILM: 5%, .25W 15 k	1	TRW/IRC	RG1/4
R26	RESISTOR, STABLE FILM: 5%, .25W 22 k	1	TRW/IRC	RG1/4
R45,48, 49,51	RESISTOR, STABLE FILM: 5%, .25W 47 k	4	TRW/IRC	RG1/4
R8	RESISTOR, STABLE FILM: 5%, .25W 100 k	1	TRW/IRC	RG1/4
R24	RESISTOR, STABLE FILM: 5%, .25W 150 k	1	TRW/IRC	RG1/4
R50,52	RESISTOR, STABLE FILM: 5%, .25W 470 k	2	TRW/IRC	RG1/4
R17,46	RESISTOR, STABLE FILM: 5%, .25W 680 k	2	TRW/CINCH	RG1/4
R47	POT, TRIM: 3/8 In End Adj, 18T 10 k	1	Beck/Heli	68XR10K
R3	POT, TRIM: RECT, 15T 5 k	1	Bourns	3006P-1-502
R55	POT, TRIM: 3/8 In End Adj. 18T 5 k	1	Beck/Heli	68XR5K
C27	CAPACITOR, DISC: 10%, 500V, Z5U 0.01 uF	1	ERIE	811-000 Z5U0 103M
C5,6	CAPACITOR, MICA, DM15: 5%, 500V 100 pF	2	El-Menco	CM05FD101J03
C12-17	CAPACITOR, MICA, DM19: 1%, 500V 3000 pF	6	El-Menco	CM06FD302F03
C1,2	CAPACITOR, AXIAL MPE: 10%, 250V .10 uF	2	Indco	2.5LUMZ10
C24	CAPACITOR, TANT ELECT: AXIAL, 10%, 10V 100 uF	1	Sprague	150D107X9010R2
C9,10,26	CAPACITOR, MONO: 10%, 50V, Z5U .10 uF	3	Sprague	7CZ5U104X0050D1
C7,8,11, 25,29	CAPACITOR, MONO: 10%, 50V, Z5U 1.0 uF	5	Sprague	7CZ5U105X005DE2
C3,4	CAPACITOR, MONO: 10%, 100V, NPD 3300 pF	2	ERIE	8131-100 C0G0 332K
C20,21	CAPACITOR, TANT, 10%, 35V, 2.2 uF	2	Cramer	TK203522510
C18,19,22, 23,28	CAPACITOR, TANT ELECT: DIP RAD, 10%, 35V 10 uF	5	ITT	TAP-F10K35

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Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
Q1	TRANSISTOR, NPN LOW NOISE	1	Fchildsemi	2N5961
Q2	TRANSISTOR, P-CHAN J-FET SWITCH	1	Siliconix	E175
CR1,2	DIODE, SIGNAL	2	GE Semi	1N4148
Q3	TRANSISTOR, N-CHAN J-FET	1	Siliconix	E112
Q4	TRANSISTOR, J-FET CURRENT REG, 430 uA	1	Siliconix	E502
U1,6,7	IC, LINEAR, DUAL GEN PUR OP AMP	3	Moto Semi	MC1458P1
U2	IC, LINEAR, DUAL OP AMP	1	Raythsemi	RC4558NB
U3,4	IC, LINEAR, VOLTAGE COMPARATOR, 8-PIN DIP	2	Nat'l Semi	LM311N
U5	IC, TTL, DUAL RETRIGGERABLE MONO	1	Nat'l Semi	DM8853N
U10	IC, LINEAR, NEG 12V +5% Reg, to-92	1	Moto Semi	MC79L12ACP
U11	IC, LINEAR, +12V +5% Reg, to-92	1	Moto Semi	MC78L12ACP
U8,9	IC, LINEAR, DUAL LOW PWR BI-FET OP AMP	2	TI Semi	TL062CP
	SOCKET	2	TRW/CINCH	16DIP
J119	HEADER, Rt Angle Post, .100 OC, 4 Pos	1	Molex	22-05-2041

PC ASSEMBLY, MOTHER BOARD - (20008009) - A28

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R1	RESISTOR, STABLE FILM: 5%, .25W 220 Ω	1	TRW/IRC	RG1/4
R2	RESISTOR, STABLE FILM: 5%, .25W 180 Ω	1	TRW/IRC	RG1/4
C1	CAPACITOR, TANT ELECT: AXIAL, 10%, 20V 10 uF	1	Sprague	150D106X902082
C2	CAPACITOR, TANT ELECT: AXIAL, 10%, 6V 180 uF	1	Sprague	150D187X9006R2
J23	HEADER, STR POST, .100 OC, 4 Pos	1	AMP	87224-4
J15,16,20, 21,22	HEADER, STR POST, .100 OC, 10 Pos	5	AMP	1-87224-0
J13,14,18	HEADER, STR POST, .100 OC, 12 Pos	3	AMP	1-87224-2
J101-108	EDGE CONNECTION, 44 Pos	8	Amphenol	225-22221-410(11
	KEYING DEVICE, BETWEEN CONTACT	16	Amphenol	225-594

PC ASSY, INTERDIGITAL TIME SELECT - (20010898) - A29

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
U2	RESISTOR NET, 10 Pin Sip, 9 Bussed 2% 22 k	1	Bourns	4301R-101-223
C1	CAPACITOR, TANT ELECT: DIP RAD, 10%, 35V 10 uF	1	ITT	TAP-F10K35
J120	HEADER, Rt Angle Post, .100 OC, 10 Pos	1	Molex	22-05-2101
U1	IC, CMOS, 8 Input NAND/AND GATE	1	RCA	CD4068BE
S1	SWITCH ASSEMBLY, PUSH BUTTON	1	Wilcom	01102557

PC ASSY, IDT CLOCK - (20724365) - PART OF A30

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
U18	IC, Cmos, Dual Prog. BCD/Binary Counter	1	Moto Semi	MC14569BCP
U19	IC, Cmos, Programmable BCD Counter	1	RCA	MC14522BCP
R11	RESISTOR, Stable Film: 5%, .25W 4.7 k	1	TRW/IRC	RG1/4
	WIRE, Hookup 22AWG (7 x 30)	A/R		

PC ASSY, KYB DECODER-STORE-CONTROL - (20010773) - A30

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
	PC ASSY, IDT CLOCK	1	Wilcom	20724365
R4,5	RESISTOR, Stable Film: 5%, .25W 22 k	2	TRW/IRC	RG1/4
R2,3, 8,9	RESISTOR, Stable Film: 5%, .25W 100 k	4	TRW/IRC	RG1/4
R7	RESISTOR, Stable Film: 5%, .25W 470 k	1	TRW/IRC	RG1/4
R6	RESISTOR, Stable Film: 5%, .25W 1 Meg	1	TRW/IRC	RG1/4
C8	CAPACITOR, Disc: 10%, 500V, 500 pF	1	ERIE	831000X5F-0501K
C2,5, 4,7, 11,12	CAPACITOR, Disc: 10%, 500V, .001 uF	6	ERIE	851000X5E-0102J
C9	CAPACITOR, Disc: 10%, 500V .005 uF	1	ERIE	811000X5R-0502K
C10	CAPACITOR, Mono, 10%, 50V 1.0 uF	1	Sprague	7CZ5V105X-005OE
C1	CAPACITOR, Dip Tant: 10%, 35V 10 uF	1	ITT	TAG-F10K35
CR1	DIODE, Signal	1	GE Semi	1N4148
U1	IC, Cmos, Keyboard Decoder	1	Motorola	MC14419
U2	IC, Cmos, Dual 4-Input Nor Gate	1	RCA	CD4002BE
U3	IC, Cmos, Quad 2-Input Nor Gate	1	RCA	CD4001BE
U4	IC, Cmos, 3 Input Nand	1	RCA	CD40106BE
U5	IC, Cmos, Dual J-K Flip-Flop	1	RCA	CD4027BE
U6	IC, Cmos, Quad D Latch	1	RCA	CD4042BE
U7	IC, Cmos, 4-Bit Data Selector	1	Motorola	MC14519BCP
U8	IC, Cmos, Presettable up/down Counter	1	RCA	CD4029BE
U9	IC, Cmos, Quad 2-Input Nand Gate	1	RCA	CD4011BE
U10	IC, Memory, 256 x 4 Static Cmos Ram	1	Intel	P5101L-3
U11	IC, Cmos, 4 Bit Comparator	1	RCA	CD4063BE
U12	IC, Cmos, Dual 4-Bit Binary Up Counter	1	Motorola	MC14520BCP
U13	IC, Cmos, 12-Stage Binary Ripple Counter	1	RCA	CD4040BE
U14,15	IC, Cmos, Quad Low-to-high Level Shifter	2	RCA	CD40109BE
U16	IC, Linear, +5V ±10%, Reg, To-92	1	Nat'l Semi	LM78L05CZ
U17	IC, Cmos, Quad 2-Input or Gate	1	RCA	CD4071BE
J115	HEADER, Rt Angle Post, .100 OC, 14 Pos	1	Molex	22-05-2141
	Wire, Hookup 22AWG (Solid)	A/R		

10.0 DIFFERENCE DATA

10.1 General

10.1.01 This section of the manual indicates information relative to changes in circuitry, operation, and features of the Model T222C Signaling Test Set.

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WILCOM PRODUCTS INC.
DANIEL WEBSTER HIGHWAY
P.O. BOX 508 LACONIA, N.H. 03246

MANUAL CHANGE INFORMATION

PRODUCT T222C
Assembly A30

ASSEMBLY Keyboard
Decoder-Store Control

CHANGE	DESCRIPTION
ECO 1123 S/N 334 & up.	This change order combines the piggy-back IDT clock, PC Assembly 207 2436 5, with the Keyboard Decoder-Store Control PC Assembly 200 1077 3 figure 8-47. The other drawings included in the change are: Parts List 200 1077 3 Schematic 500 0612 1 figure 8-48 The revised drawings for units with serial numbers 334 and up are shown below and on the following two pages.

PC ASSY, KYB DECODER-STORE-CONTROL - (20010773) - A30

Ref. Desig.	Description	Qty.	Mfr.	Manufacturer's Number
R1	RESISTOR, Stable Film: 5%, .25W 4.7 k	1	TRW/IRC	RG1/4
R4,5	RESISTOR, Stable Film: 5%, .25W 22 k	2	TRW/IRC	RG1/4
R2,3,8,9	RESISTOR, Stable Film: 5%, .25W 100 k	4	TRW/IRC	RG1/4
R7	RESISTOR, Stable Film: 5%, .25W 470 k	1	TRW/IRC	RG1/4
R6	RESISTOR, Stable Film: 5%, .25W 1 Meg	1	TRW/IRC	RG1/4
C9	CAPACITOR, Disc: 10%, 500V, X5F 500 pF	1	ERIE	831-000 X5FO
C2-8	CAPACITOR, Disc: 10%, 500V, X5E .001 uF	7	ERIE	851-000 X530 102J
C10	CAPACITOR, Disc: 10%, 500V, X5R .005 uF	1	ERIE	811-000 X5RO 502K
C11	CAPACITOR, Mono: 20%, 50V, Z5U 1.0 uF	1	Sprague	7CZ5U105-XOO5OE2
C1	CAPACITOR, Tant Elect: Dip Rad, 10%, 35V 10 uF	1	ITT	TAP-F10K35
D1	DIODE, Signal	1	GE Semi	1N4148
U1	IC, Cmos, Keyboard Decoder	1	Moto Semi	MC14419P
U2	IC, Cmos, Dual 4-Input Nor Gate	1	RCA	CD4002BE
U3	IC, Cmos, Quad 2-Input Nor Gate	1	RCA	CD4001BE
U4	IC, Cmos, Hex Inverter, Schmitt	1	RCA	CD40106BE
U5	IC, Cmos, Dual J-K Flip-Flop	1	RCA	CD4027BE
U6	IC, Cmos, Quad D Latch	1	RCA	CD4042BE
U7	IC, Cmos, 4-Bit Data Selector	1	Moto Semi	MC14519BCP
U8	IC, Cmos, Presettable up/down counter	1	RCA	CD4029BE
U9	IC, Cmos, Quad 2-Input Nand Gate	1	RCA	CD4011BE
U10	IC, Memory, 256 x 4 Static Cmos Ram	1	Intel	P5101L-3
U11	IC, Cmos, 4 Bit Comparator	1	RCA	CD4063BE
U12	IC, Cmos, Dual 4-Bit Binary up counter	1	Moto Semi	MC14520BCP
U13	IC, Cmos, 12-Stage Binary Ripple Counter	1	RCA	CD4040BE
U14,15	IC, Cmos, Quad Low-to-High Level Shifter	2	RCA	CD40109BE
U16	IC, Linear, +5V +5% Reg, to-92	1	Nat'l Semi	LM78L05ACZ
U17	IC, Cmos, Quad 2-Input or Gate	1	RCA	CD4071BE
U18	IC, Cmos, Dual Prog. BCD/Binary Counter	1	Moto Semi	MC14569BCP
U19	IC, Cmos, Programmable BCD Counter	1	Moto Semi	MC14522BCP
J115	HEADER, Rt Angle Post, .100 OC, 14 Pos	1	Molex	22-05-2141

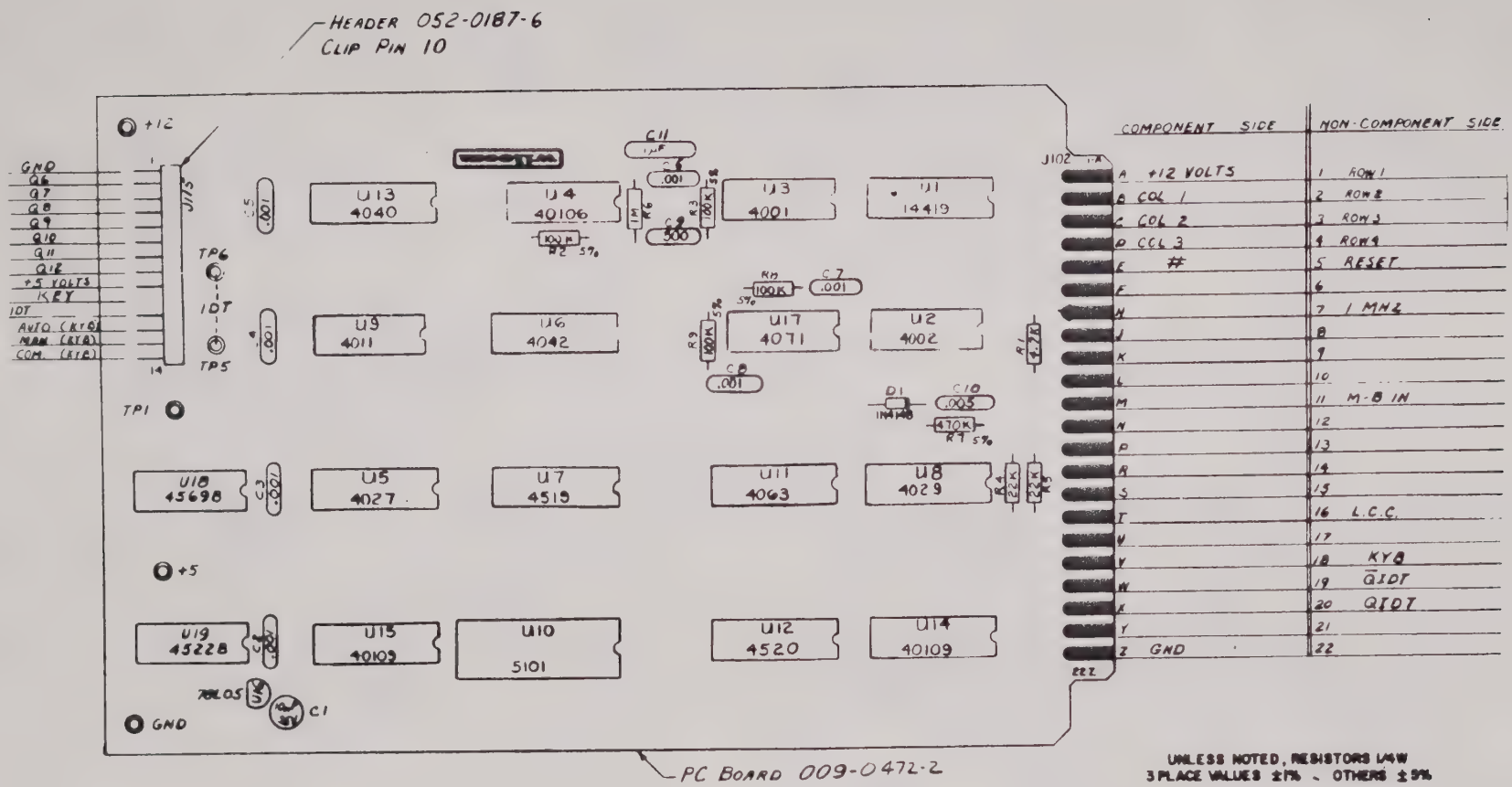

FIGURE 8-47
Keyboard-Decoder-Store Control
PC Assembly A30

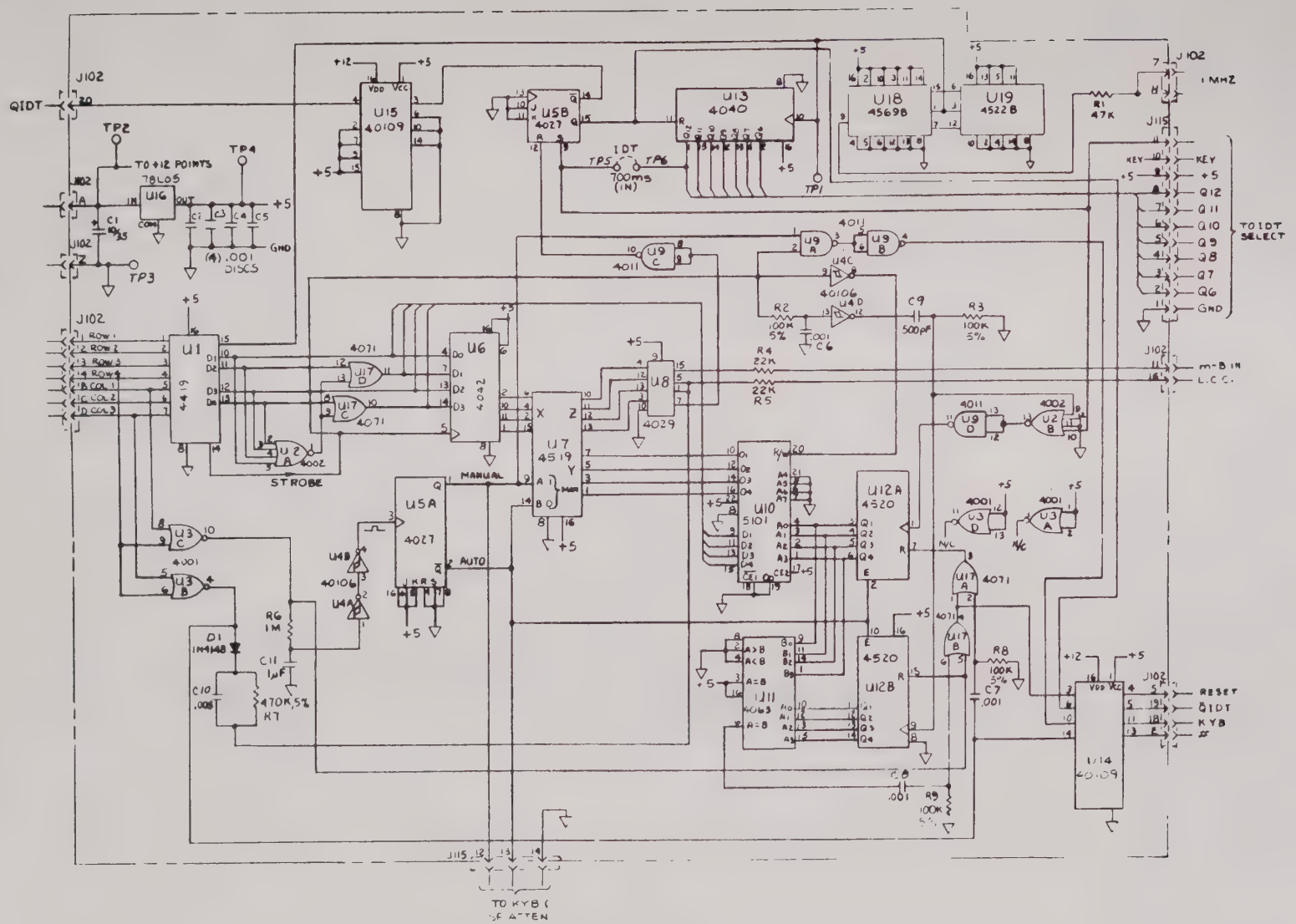

FIGURE 8-48
Keyboard-Decoder-Store Control
Schematic A30

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MANUAL CHANGE INFORMATION

PRODUCT T222C
Assembly A27

ASSEMBLY SF Send
Receive Detector

CHANGE	DESCRIPTION
ECO 1127 S/N 334 & up.	PC Assembly 200 1090 6 has been revised to include the Piggyback Assembly shown in figure 8-42 page 8-44. The revised drawing is shown below

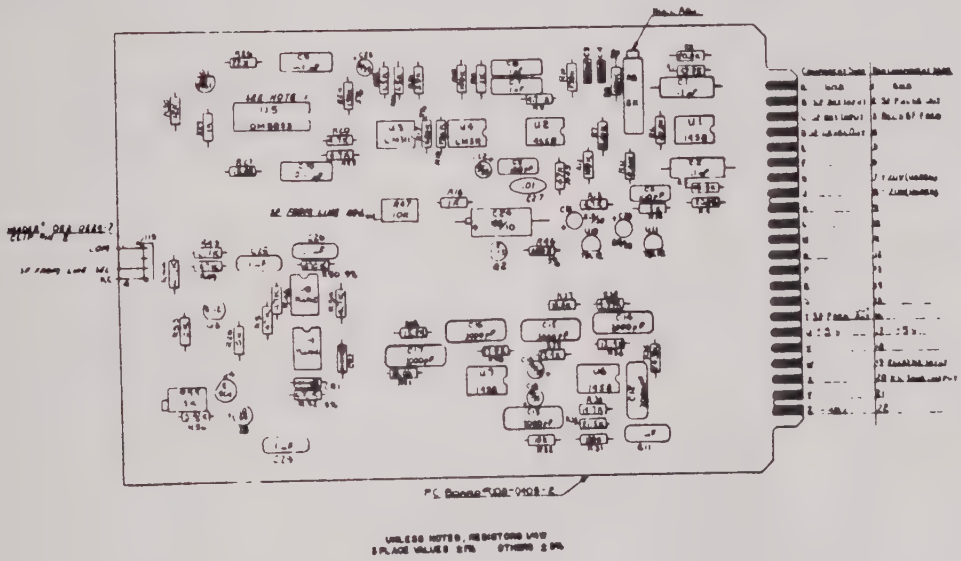

FIGURE 8-42
SF Send Receive Detector
PC Assembly A27

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DANIEL WEBSTER HIGHWAY
P.O. BOX 508 LACONIA. N.H. 03246

MANUAL CHANGE INFORMATION

PRODUCT T222C

ASSEMBLY Keyboard & S.F. Attenuator

CHANGE	DESCRIPTION
ECO 1262 S/N 375 and above	CAPACITOR C4 added between J28 pin four and U1 pin 7.

PARTS LIST:

PC ASSEMBLY, KEYBOARD & S.F. ATTENUATOR - (20010831) - A15

Ref. Desig	Description	Qty.	Mfr.	Manufacturer Number
C4	CAPACITOR MONO: 20%, 50 V., 1.0μF	1	Sprague	7CZ5U105x0050E2

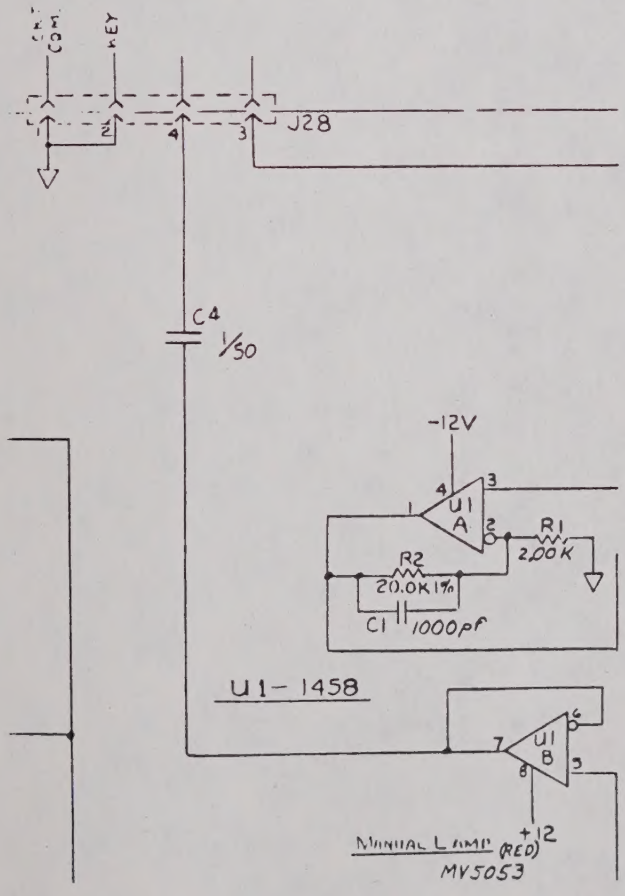

FIGURE 8-21
Keyboard & S.F. Attenuator
Schematic A15

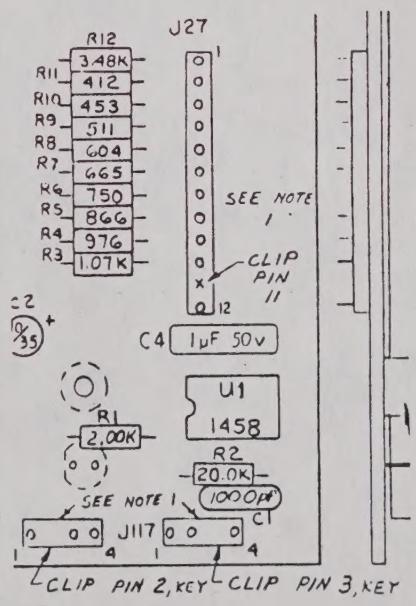

FIGURE 8-22
Keyboard & S.F. Attenuator
PC Assembly A15